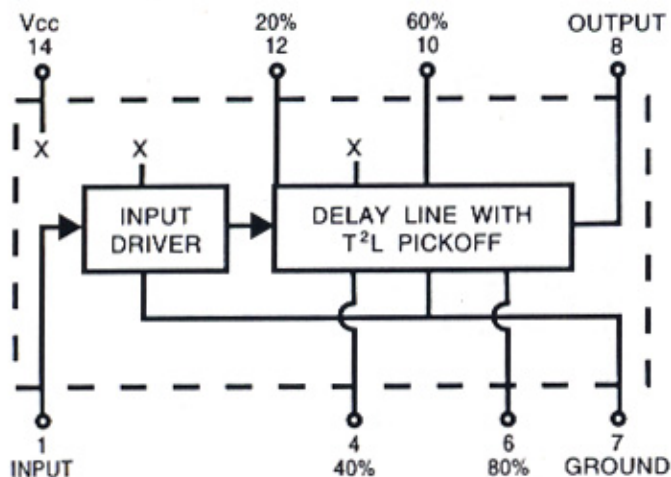


BLOCK DIAGRAM IS SHOWN BELOW



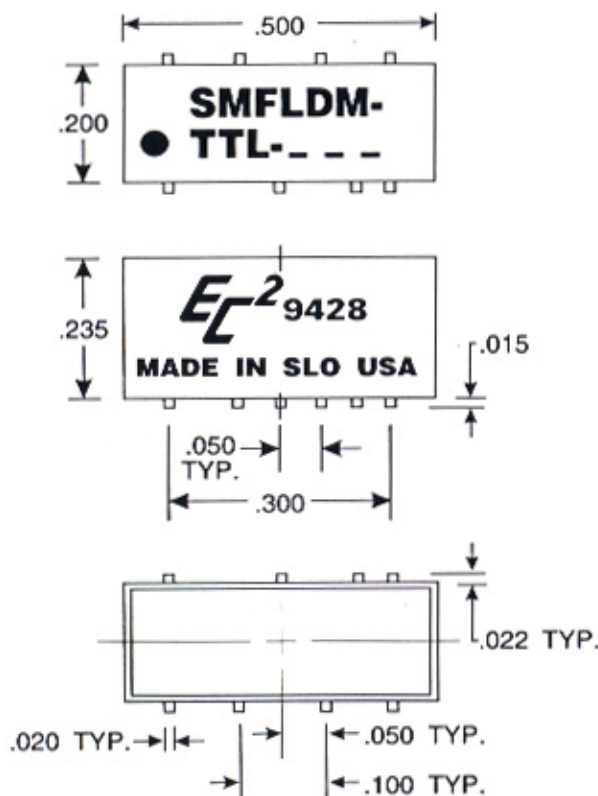
OPERATING SPECIFICATIONS

* V _{CC} supply voltage:	4.75 to 5.25V DC
V _{CC} supply current:	
Constant "0" in	40mA typical
Constant "1" in	7mA typical
Logic 1 Input:	
Voltage	2V min.; V _{CC} max.
Current	2.7V = 20uA max. 5.5V = 1mA max.
Logic 0 Input:	
Voltage	.8V max.
Current	-.6mA max.
Logic 1 Voltage out:	2.7V min.
Logic 0 Voltage out:	.5V max.
Operating temperature range:	0 to 70°C.
Storage temperature:	-55 to +125°C.

* Delays increase or decrease approximately 2% for a respective increase or decrease of 5% in supply voltage.

MECHANICAL DETAIL IS SHOWN BELOW

PART NUMBER TABLE



φ DELAYS AND TOLERANCES (in ns)					
PART NO.	Tap 1	Tap 2	Tap 3	Tap 4	OUTPUT
SMFLDM-TTL-10	6 ± 1	7 ± 1	8 ± 1	9 ± 1	10 ± 1
SMFLDM-TTL-12	6 ± 1	7.5 ± 1	9 ± 1	10.5 ± 1	12 ± 1
SMFLDM-TTL-14	6 ± 1	8 ± 1	10 ± 1	12 ± 1	14 ± 1
SMFLDM-TTL-16	6 ± 1	8.5 ± 1	11 ± 1	13.5 ± 1	16 ± 1
SMFLDM-TTL-18	6 ± 1	9 ± 1	12 ± 1	15 ± 1	18 ± 1
SMFLDM-TTL-22	6 ± 1	10 ± 1	14 ± 1	18 ± 1	22 ± 1
SMFLDM-TTL-25	5 ± 1	10 ± 1	15 ± 1	20 ± 1	25 ± 1
SMFLDM-TTL-30	6 ± 1	12 ± 1	18 ± 1	24 ± 1	30 ± 1
SMFLDM-TTL-35	7 ± 1	14 ± 1	21 ± 1	28 ± 1.5	35 ± 1.5
SMFLDM-TTL-40	8 ± 1	16 ± 1	24 ± 1.5	32 ± 1.5	40 ± 1.5
SMFLDM-TTL-45	9 ± 1	18 ± 1	27 ± 1.5	36 ± 1.5	45 ± 2
SMFLDM-TTL-50	10 ± 1	20 ± 1	30 ± 1.5	40 ± 2	50 ± 2
SMFLDM-TTL-55	11 ± 1	22 ± 1	33 ± 1.5	44 ± 2	55 ± 2
SMFLDM-TTL-60	12 ± 1	24 ± 1	36 ± 1.5	48 ± 2	60 ± 2
SMFLDM-TTL-65	13 ± 1	26 ± 1.5	39 ± 1.5	52 ± 2	65 ± 2.5
SMFLDM-TTL-70	14 ± 1	28 ± 1.5	42 ± 2	56 ± 2	70 ± 2.5
SMFLDM-TTL-75	15 ± 1	30 ± 1.5	45 ± 2	60 ± 2.5	75 ± 2.5
SMFLDM-TTL-80	16 ± 1	32 ± 1.5	48 ± 2	64 ± 2.5	80 ± 3
SMFLDM-TTL-85	17 ± 1	34 ± 1.5	51 ± 2	68 ± 2.5	85 ± 3
SMFLDM-TTL-90	18 ± 1	36 ± 1.5	54 ± 2	72 ± 2.5	90 ± 3
SMFLDM-TTL-95	19 ± 1	38 ± 1.5	57 ± 2	76 ± 2.5	95 ± 3
SMFLDM-TTL-100	20 ± 1	40 ± 1.5	60 ± 2	80 ± 3	100 ± 3
SMFLDM-TTL-125	25 ± 1	50 ± 2	75 ± 2.5	100 ± 3	125 ± 4
SMFLDM-TTL-150	30 ± 1.5	60 ± 2	90 ± 3	120 ± 4	150 ± 5
SMFLDM-TTL-175	35 ± 1.5	70 ± 2.5	105 ± 4	140 ± 5	175 ± 5
SMFLDM-TTL-200	40 ± 1.5	80 ± 2.5	120 ± 4	160 ± 5	200 ± 6
SMFLDM-TTL-225	45 ± 2	90 ± 3	135 ± 4	180 ± 6	225 ± 7
SMFLDM-TTL-250	50 ± 2	100 ± 3	150 ± 4.5	200 ± 6	250 ± 8

TEST CONDITIONS

- All measurements are made at 25°C.
- V_{CC} supply voltage is maintained at 5.0V DC.
- All units are tested using a FAST toggle-type positive input pulse and one FAST T²L load at the output being tested.
- Input pulse width used is 5 to 10ns longer than full delay of module under test; spacing between pulses (falling edge to rising edge) is three times the pulse width used.

φ All modules can be operated with a minimum input pulse width of 40% of full delay and pulse period approaching square wave; since delay accuracies may be somewhat degraded, it is suggested that the module be evaluated under the intended specific operating conditions. [Special modules can be readily manufactured to improve accuracies and/or provide customer specified random delay times for specific applications.](#)