0.1 The Pace Maker

For reference, I here describe the initial version of the bunch counter. This desing is bugged: if a L1A comes before the 2nd B0 marker after h-r-r, the counter is still not in synch. The reason is that the counter only starts after the 1st B0 marker, and despite the complicated logic described below, it takes at least 2 B0 markers to properly synch.

On schematic sheet 6, right next to the heart is the **Bunch_Counter**, Dirac's pacemaker. Sheet 7 contains the **Bunch_Counter** logic. On the right side of the sheet is the standard **DAQ** L1 FIFO and L2 Buffer for the **BUNCH** data. **BUNCH** counts the number of clocks from an interaction for the event. As data is clocked into the L1 FIFOs around Dirac, the **BUNCH** chip is also clocking data into its L1 FIFO. In this way, if there is a clock distribution problem anywhere in the system, we can quickly diagnose and solve the problem. In TRIGMON, the online trigger monitoring software, the data from all trigger boards will be checked to insure that they all have the same bunch number. Pretty simple!

The schematic for the **BUNCH** chip is called OLDBC.GDF (see OLDBC.ps for a PS version). In essence, the **BUNCH** chip is a counter with a shift register as the on/off switch. The counter is located on the far right of the schematic and the shift register on the far left. The shift register is reset by the a **_B0** signal. The **_B0** pulse indicates the occurance of a special bunch, logically called number 0. Equally logically, we reset the counter on this pulse, suitably delayed by our depth in the pipeline. The SR is clocked by the L1 FIFO WCLK signal, **L1SI**. The **_RESET** signal pre–sets the SR to prepare it for a **_B0**. Only 8 taps from the SR are used, the others are just place holders. So prior to actual data taking, the approximate postion of Dirac in the pipeline must be known, 8 clocks is a lot of lee–way. **BUNCH** has a 3–bit register called **Bunch Offset** in the memory map. This register picks which of the 8 SR taps are used to clear the counter. The 8–1 multiplexer in the center of the schematic has the 3–bits from the register as an address and the 8 SR taps from which to pick. Watch the next step, it's a lu–lu.

The logic to actually clear the counter is difficult. During a startup sequence, a **_RESET** must come while **_halt** is asserted. On **BUNCH**, these signals are ORed to clear a flip–flop. When the system starts running the flip–flop(FF) is initally cleared. The D input is GND and the clock is the output of the SR. Thus, when the correct tap is turned on, the FF will be clocked to GND. The key is the pre–set for the FF. This includes a little feedback logic. First, on a proper startup sequence reset, another FF is pre–set. The output of this FF drives the pre–set of the initial FF. So at startup, the first FF is low and the second is high. The output of the first FF feeds back to pre–set the second FF if the first one goes high. If the SR is low, then the clock to the second FF is blocked. The transition of the SR from low to high triggers the actual reset of the counter. The first effect is to clock the first FF which resets the counter. There is a slight danger at this point; if a **L1SI** rising edge occurs during the transition of the first FF and clearing of the counter, then a race condition occurs. This could cause a failure to reset the counter. Be aware. Now the rising edge of the next **L1SI** will turn on the first FF, allowing the counter to start. The falling edge of the same **L1SI** counts to 1. Read technical note 6. And we are off to the races.

As per CDF specification, the first word of DAQ readout contains the bunch counter number, board ID and serial numbers.[12] In the lower middle of schematic sheet 6 are a series of jumpers that set the board ID [1] (S2) and serial numbers (S1). These are placed on the board during stuffing of the components. The actual selection of these bits during DAQ readout is part of the memory map. A reported [1] feature of the switches S1 is apparent on the schematics: the switch counting goes as 1 2 3 4 5 6 9 7 8 10, instead of 1 2 3 4 5 6 7 8 9 10. Therefore: to set bit 6 (staring counting at 0) must set switch number 9 (starting counting at 1). To set bit 7, must set switch number 7; to set bit 8, switch number 8.

[1]Dirac board ID is 005 (decimal)

References

[1] Wahl, John E. and Amaral, Pedro *Dirac — The FINAL Specificaton.* CDF/DOC/TRIGGER/CDFR/4225.

[2] Shaw, Teresa M. *Specification for ADC/Memory Module.* Particle Physics Division. CDF Upgrade Project. 6/11/97.

[3] Freeman, Jim, et al. *The Run II eXtrememly Fast Tracker (XFT)* http://cdfsga.fnal.gov/upgrades/daq_trig/xft/xft_home.html.

[4] Toback, Dave. *Crate Sum - Upgrade for Run II.* CDF Trigger Note 91.

[5] The P3 Auxilliary(AUX) card was designed and built by Peter Wilson.

[6] Sarah Truitt is designing the Digital Compare and Sum (DCAS) boards for the Level 2 trigger.

[7] CDF Group, Yale University. *Trigger Supervisor Protocols for Run II* August 18, 1996, Version 1.2.

[8] CDF DAQ Group. *The CDF DAQ Manager's Handbook.* August 18, 1996, Draft #3.

[9] Wahl, John and Wilson, Peter J. *Digital Receive And Compare (DIRAC) Board Startup Timing Diagram.* June 11, 1995, CDF Trigger Note 95.

[10] Peterson, Wade D. *The VMEbus Handbook.* Third Edition. VITA. Scottsdale, AZ, 1993.

[11] VIPA *VME-P Document.* NIM/VME-P 9612.

[12] Ohl, K, Wahl, J, and Wilson, P. *Specification of DAQ/Trigger Synchronization Checking Protocol and VME board Header word.* Version 2.0. CDF/DOC/TRIGGER/CDFR/3145.

[13] Altera Corporation. *Bit Blaster Serial Download Cable Data Sheet.* Altera Corporation Product Data Sheet.