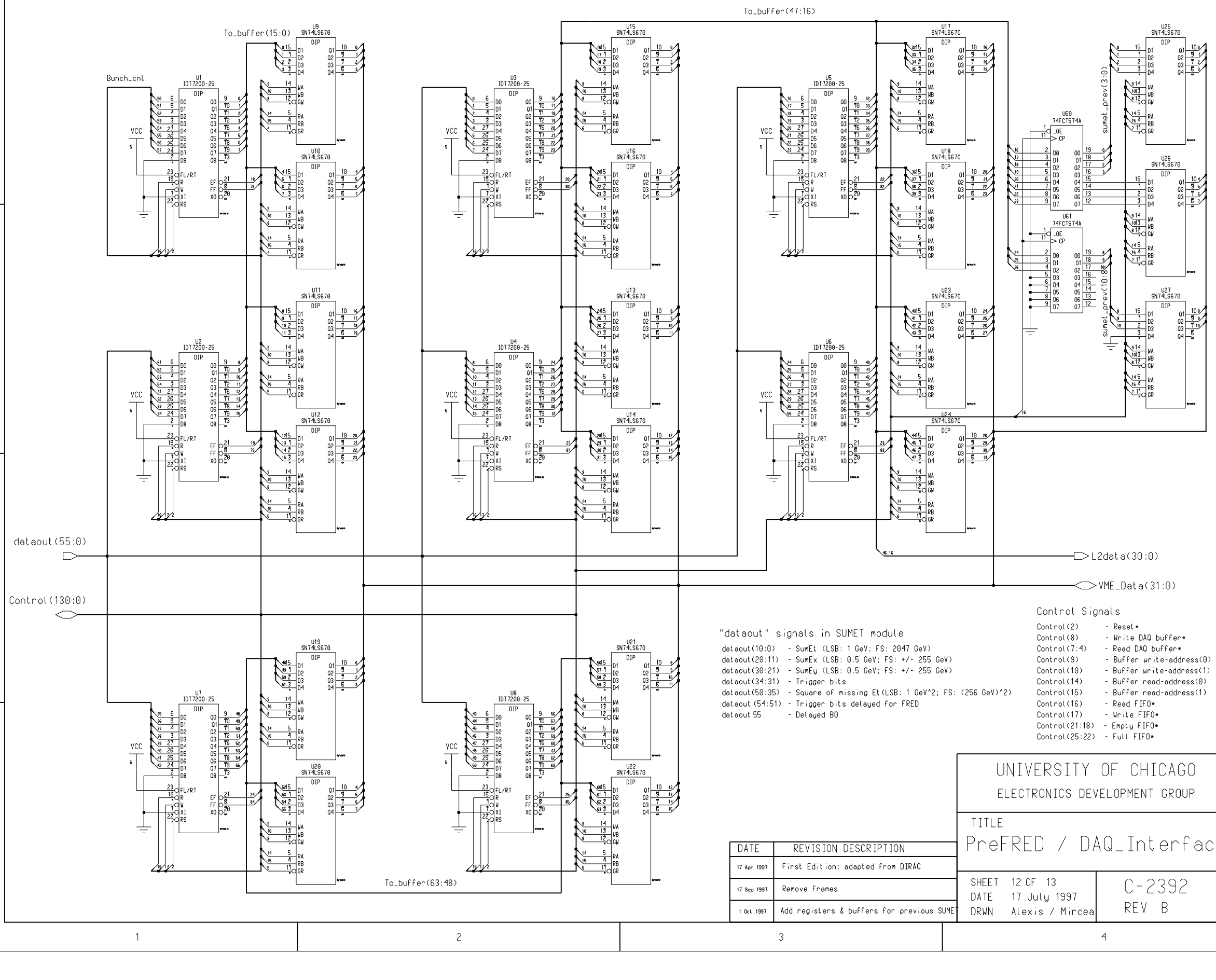

"dataout" signals in SUMET module

dataout(10:0)	- SumEt (LSB: 1 GeV; FS: 2047 GeV)
dataout(20:11)	- SumEx (LSB: 0.5 GeV; FS: +/- 255 GeV)
dataout(30:21)	- SumEy (LSB: 0.5 GeV; FS: +/- 255 GeV)
dataout(34:31)	- Trigger bits
dataout(50:35)	- Square of missing Et(LSB: 1 GeV^2; FS: (256 GeV)^2)
dataout(54:51)	- Trigger bits delayed for FRED
dataout 55	- Delayed B0

Control Signals

Control(2)	- Reset*
Control(8)	- Write DAQ buffer*
Control(7:4)	- Read DAQ buffer*
Control(9)	- Buffer write-address(0)
Control(10)	- Buffer write-address(1)
Control(14)	- Buffer read-address(0)
Control(15)	- Buffer read-address(1)
Control(16)	- Read FIFO*
Control(17)	- Write FIFO*
Control(21:18)	- Empty FIFO*
Control(25:22)	- Full FIFO*

DATE	REVISION DESCRIPTION
17 Apr 1997	First Edition: adapted from DIRAC
17 Sep 1997	Remove frames
1 Oct 1997	Add registers & buffers for previous SUMET

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
PreFRED / DAQ_Interface

SHEET 12 OF 13
DATE 17 July 1997
DRWN Alexis / Mircea

C-2392
REV B