Data Transceivers

U30
SN74ABTE16245

U31
SN74ABTE16245

U74
74FCT1541

U73
74FCT1541

U72
74FCT1541

U75
74FCT1541

U51
SN74BCT760
DIP
NULL

U8
EPM7128S-160-7
TLP

VMEbus_P1
Sheet 3.
Data(15:0)
Address(23:1)
AM(5:0)
VME_P1(159:0)
BR(3:0)
BGIN(3:0)
BGOUT(3:0)
IRQ(7:1)
GA*(4:0)
VME_Controls(17:0)
15:0
7
8
IACK

VMEbus_P0
Sheet 4.
VME_P0(94:0)

P2_CUSTOM
Sheet 5.
Data(31:16)
Address(31:24)
VME_P2(159:0)
Trig_Ctrl(38:0)
31:16

VME_P1(159:0)
VME_P0(94:0)
VME_P2(159:0)

TDI
TMS
TDO
TCK
SYSCLK
_AS
_DTACK
_BERR
_ACK
_DS1
_DS0
_LWORD
vme_write
_vme_err
vme_write
dir_trans
_vme_data_str
A(31:1)
D(31:0)
R24 390
R25 390
VCC

VME_Data(31:0)
GA(4:0)
VME_Address(26:2)
VME_Control(7:0)
VME_config(9:0)
Trig_Ctrl(38:0)

/net/mentor/designs/CDF_L1/final_PreFRED/PreFRED2/mcf/VME_Interface.mcf

Trig_Ctrl are signals sent
along the user defined pins
of P2 for Global signals
sent throughout the trigger.
NOTE: Be sure to buffer
any P2 signals going to more than
one chip on the board, so that
the tracer doesnt get overloaded.

DATE	REVISION DESCRIPTION
16 Dec 93	Original design -- YF
18 Nov 96	3rd Prototype - Bug Fixes -- JW
10 Oct 97	Replace VME2000 & other with single PLD

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
PreFRED / VME Interface

SHEET 2 OF 13
DATE 12 May, 1999
DRWN alexis / mircea

C-2392
REV B