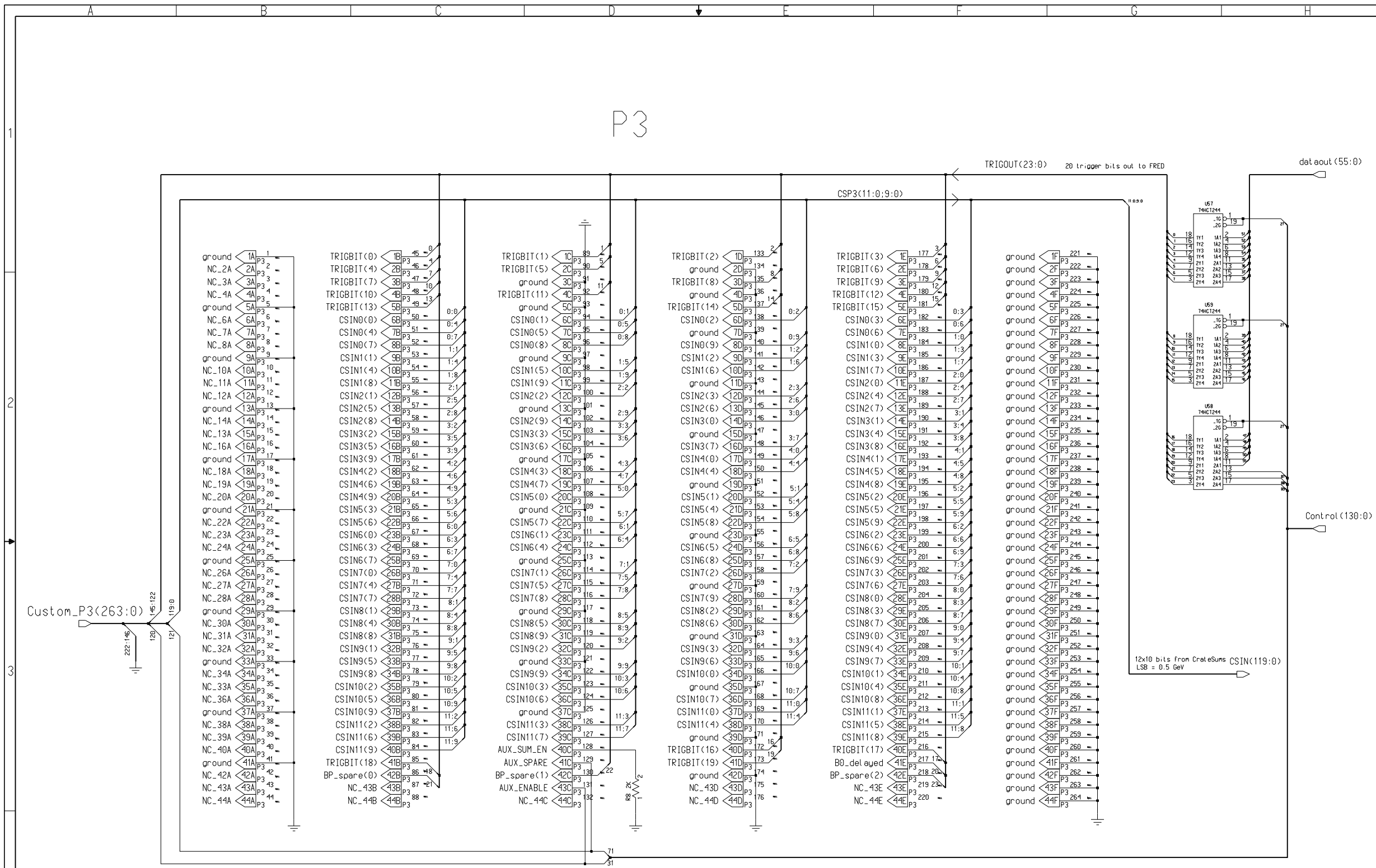

Note: z-row is missing because it appears only on backplane.

Channel 0 of CSIN corresponds to wedges 0 and 1, channel 1 corresponds to wedges 2 and 3, etc.

Note: End-wall summing irrelevant here, therefore disabled by setting AUX_SUM_EN to GND.

DATE	REVISION DESCRIPTION
18 Feb 97	Customized for PreFRED modules
30 Oct 97	Added B0_delayed and spare bits to FRED

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
PreFRED / Custom_P3

SHEET 9 OF 13
DATE 18 Feb 97
DRWN Alexis Amadon

C-2392
REV B