Background

The COT has 2520 cells with 12 sense wires per cell for a total of 30,240 readout channels. The cells are arranged in 8 super-layers, referred to as SL1–SL8, with a varying number of cells per superlayer. SL1, the inner most superlayer, has 168 cells; while SL8, the outer most, has 480 cells.

There is one ASD (Amplifier Shaper Discriminator) board per two cells, for a total of 1260 ASD boards. Each ASD board has 3 ASDQ chips (the Q denotes a version that measures charge). Each ASDQ chip has one analog monitor output which looks at the output of the BLR (Base Line Restorer) circuit. The output is an open-collector differential pair that is enabled by adding pull-up resistors. At present, each daughter board has only one analog output brought to an output connector. However, it is straightforward to access the other outputs. Thus there are a total of 3780 analog monitor outputs available.

Differential output voltages from the analog monitor, going into 40Ω per leg, are ~1.5 mV r.m.s. noise, and ~50 mV peak for Fe^{55} pulses at nominal chamber gain. Signals from tracks have a wide variation due to variation in charge deposition from geometry (polar and aspect angle) as well as fluctuations in ionization rate. A reasonable reference point is the typical signal for a minimum ionizing track, going at 90° to the drift direction and to the wires; this is ~1/3rd that of Fe^{55} or ~17 mV.

The ASDQ measures total charge of input pulses using a variant of a dual-slope ADC technique to convert integrated charge to pulse width. The pulse width (as well as start time) is recorded by TDCs on the End Walls. The input pulse to the ASDQ has very large variations in shape, as well as total amplitude, due to the intrinsic properties of ionization, drift, and gas gain; it is difficult to simulate this accurately. A lot of work has gone into optimizing the chip to measure total charge independent of pulse shape, and to minimize the affect of preceding pulses on measured charge. However, we need to more accurately quantify the behavior of the chip using real tracks.

The ASDs use six externally supplied voltages to control various aspects of the chip behavior. The control voltages are set by DACs independently for each "quadrant" of each superlayer. A quadrant is a 90° region of cells, by convention called A–D. Cells with their nominal center point at $0° \leq \varphi < 90°$ are in quadrant A, $90° \leq \varphi < 180°$ in quadrant B, etcetera. Low voltage power for the ASDs is also by quadrant. However, power cabling and buffering of control voltages is by octant for the five outer superlayers. Although normally we do not use separate high voltage power supplies per quadrant, the cabling is arranged to allow control at the quadrant level. So, a quadrant is a natural unit in which to do monitoring, and it is desirable to monitor at least a one channel in each octant of the outer superlayers.

Readout electronics (ASDs at the chamber, TDCs at the End Walls), besides being divided by quadrant, are split East and West. Readout of SL1, 4, 5, and 8 are on the East side; SL2, 3, 6, and 7 are on the West. Thus for readout purposes there are eight "quadrants:" Four each East and West. It is somewhat difficult and risky (in terms of ground loops) to cross quadrant boundaries; it is even more so to do an East-West crossover.

The plan, driven by available cable and cable space, is to bring out a small subset of the analog signals using micro-coax cable left over from the cancelled CTC upgrade. The cable is ~0.031″ OD with Teflon® as both the inner dielectric and outer insulation.[1] The cable impedance is ~40Ω. Groups of 25 coaxial lines are made into a ribbon using a nylon weave. Historically, this "ribbon" is called a micro-coax cable, while the term "line" to refers to single coaxial cable within the ribbon (note a "line" has two conductors). Each cable will carry 12 channels out (two lines per channel), with one unused line. We will have one cable per quadrant for a total of 96 channels brought out.

Minimal Plan

The principal (only) advantage of this plan is simplicity. I think we should keep this in mind as a fallback plan. I hope nobody asks me to defend it further. Beyond that, its only purpose here is to define the geometry of the system.

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[1] Include gauge of wires, and attenuation properties.

Cabling at the COT

Distribution of the 12 channels across each quadrant is based on several considerations.

- Minimize non-radial length of cable across the chamber face
  (makes access under the Faraday cage easier).
- Form a narrow “pie” slice
  (allows a jet trigger to selectively populate the sampled cells with high track density).
- Look for local correlation in noise.
- Sample all octants.

To meet this goals we will run the analog monitor cable along radial lines at 45°, 135°, 225°, and 315° (the octant boundaries). Since not all quadrants of cable slots available at these angles, we will need to run around the outer circumference of the COT from the nearest available slot to the desired. We will connect to the inner, middle, and outer analog monitor point for three consecutive boards in each superlayer. The table of cells and monitor points for each superlayer is given below.

	Quad A			Quad B			Quad C			Quad D		
SL	Outer (Wire 3)	Middle (Wire 7)	Inner (Wire 11)	Outer (Wire 3)	Middle (Wire 7)	Inner (Wire 11)	Outer (Wire 3)	Middle (Wire 7)	Inner (Wire 11)	Outer (Wire 3)	Middle (Wire 7)	Inner (Wire 11)
1	19	21	23	61	63	65	103	105	107	145	147	149
2	23	25	27	71	73	75	119	121	123	167	169	171
3	29	31	33	89	91	93	149	151	153	209	211	213
4	35	37	39	107	109	111	179	181	183	251	253	255
5	41	43	45	125	127	129	209	211	213	293	295	297
6	47	49	51	143	145	147	239	241	243	335	337	339
7	53	55	57	161	163	165	269	271	273	377	379	381
8	59	61	63	179	181	183	299	301	303	419	421	423

At the chamber face, we “peel off” pairs of micro-coax lines to go to the daughter board of interest. Pairs are soldered directly to 4-point, 0.1″×0.1″ modular connectors. (IDCs and crimp connections don’t work well on these wires.) We do not attempt to match cable length across superlayers, resulting in a ~2′ variation. We leave a fairly large hole in the Faraday cage, ~1/2″, so we can connect and disconnect without removing any part of the Faraday cage. We use no break in the cable on the COT face.

After a 17–23′ run each micro-coax ends at a termination board and connector left over from the CTC. The connector is 0.1″ spacing double-row suitable for plugging into .025″ square pin headers.

Passive Analog Repeater Board

The termination board plugs into a board – could be a kludge card – with twelve 1:1 pulse transformers. We have such transformers, made by Pulse Engineering (part number PE8104 — now obsolete), packaged as four independent transformers in a16-pin DIP. The output side of the transformer goes through a 30Ω resistor to match impedance to 50Ω output cable, and then to 0.1″ spacing double-row output header.

This repeater board would reside in the same region as the COT digital repeater boards, just outside the 30° conical section. It would mount to the repeater board cooling plate with quarter-turn screws. For this to work the board must have the same approximate outline as a repeater board.

Patch Panel

We have (at least) six foamed polyethylene cables, three each on East and West, available for sending analog signals to the 2nd floor. These are spares from the calibration system; they are not matched in length and may not be trimmed. The cables are most readily accessed at the top north corners. The purpose of the patch panels is to select which of the 96 analog signals are made available upstairs.

We will use cable left over from the CTC to connect the analog repeater board to a set of patch panels. This is a ribbon of 26 coax lines, with each line electrically similar to RG174 (26AWG, ~100 Ω/ft inner conductor; braided outer conductor, ~10 mΩ/ft) but with 56Ω impedance. We need to strip off one line to generate 25-line ribbons. (Unlike the micro-coax, removing one line from this cable is straightforward.)

Twelve lines will be used to bring analog signals to the patch panels; the remaining thirteen are reserved for supplying power to the active repeater board.

Each quadrant will use a ~20′ length of this cable to reach a "1^{st} stage" patch panel at each corner of the detector (eight 1^{st} stage patch panels total, 96 cables total). Three cables continue from each of these patch panels to a "2^{nd} stage" patch panel at the top north corner of each side (24 cables total). These cables are of varying length, the ones from the top north corner being a few inches while the bottom south is of order 50′. This allows sending any three of the twelve signals at each quadrant to the 2^{nd} stage patch panels. The 2^{nd} stage patch also has twelve inputs, three each from each quadrant; it allows sending any three of these to the 2^{nd} floor.

The 1^{st} and 2^{nd} stage patch panels are electrically and mechanically identical. The are simply 12 BNC feed-throughs with inputs semi-permanently connected at the back, and three cables output cables connected to the front. Unused lines should be terminated.

Improvements

This is intended to be a series of evolutionary changes. It is not necessary that we actually assemble all parts of the minimal plan in advance. It is necessary to allow time for completing the minimal plan if some of the boards described below are not likely to be completed

Active Analog Repeater Board

The pulse transformer needs a reasonably large inductance to transfer a pulse without artificially shortening the trailing edge. Unfortunately this also gives capacitive coupling which degrades the common mode rejection at high frequencies. Also, the signal from the ASD is very small (of order 10 mV) to send reliably over 250′ total run. Finally, an active device here allows cable-compensation early in the chain.

We will use a Maxim MAX4145 as an active receiver/amplifier in place of the pulse-transformers. Mechanical constraints and input/output connections are as for the transformer board. We expect to have a gain of 5 V/V (10 V/V gain on the amplifier followed by a ÷2 from series-termination) raising the nominal pulse to ~85 mV. The board will include a bias correction trim resistor that will be used to remove any DC bias on the output. A schematic is given in the appendix.

Multiplexer

The patch panel requires access to the detector in order to change which channels are available upstairs. With access to the detector, working on patch panels near the top of the detector requires a lift, which in turn requires the CMX chambers be moved. A remote controlled multiplexer is more flexible and convenient.

We plan to use an Analog Devices AD8110 16in×8out video cross-point chip to replace the patch panels. The chip includes input and output buffers. These will be controlled by a serial line coming from the 2^{nd} floor; the chip has built-in serial control logic. The control cable is a 2-pair audio cable with each pair having a foil shield. (It's what we had on hand … fortunately we don't need any speed on this line.) Tentatively we plan on using thumb-wheel switches as the "user interface" and a parallel-to-serial circuit to transmit the setting downstairs, although if a PC is handy it might be a more convenient way to go.

We need a total of 10 multiplexer boards: Eight 1^{st} stage multiplexers, and two 2^{nd} stage multiplexers. All boards will be identical, with 12 inputs and 3 outputs. The chip has unity gain; including series-termination the signal will be attenuated by a factor of two. (The AD8111, with a 2 V/V gain, would be better but is not available in time. If noise is a problem we may consider switching to this later. The board is compatible with either chip.)

To eliminate the need to design another PC board, we will duplicate the Analog Device's evaluation board, but leave out connectors we do not need: Only twelve inputs and 3 outputs will be brought to a front panel.

VME FADC boards

For d*E*/d*x* calibration and more detailed understanding of 2-track resolution, we need to correlate the analog signal with track information, e.g. to look at pulses coming from known particles (muons, electrons, and with knowledge of the 3-momentum). This requires being able to match the analog signal with data taken by the TDC. This is not possible with a scope, except using very low rate special triggers. Given the small fraction of the chamber instrumented for analog readout (96 out of 30,240 channels), it is unrealistic to expect this approach to yield a significant sample of hits from known particles.

We would like to add VME FADC boards to the TDC crates to get analog information directly into the event stream. The current plan is to have a 4- or 6-channel board, so we would need a total of two or three slots at each corner of the detector.

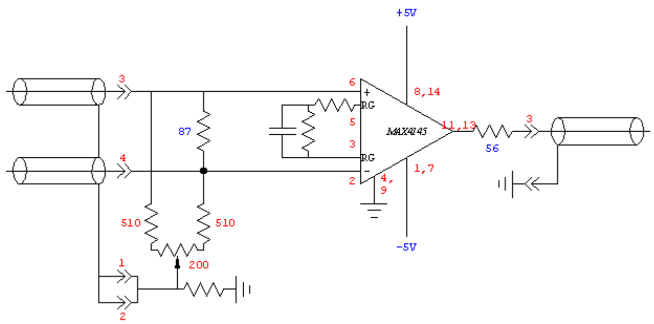
The bottom northeast corner only has two slots available; if we go with 4-channel boards we would only be able to read out 8 channels in this quadrant. All other corners have at least three empty slots.

The FADC is expected to have a high impedance receiver for each signal line. When the FADC is ready, the signal from the analog repeater board can go past the FADC with a T and continue to the multiplexer. The FADC board should have the option of terminating the line in case we wish to use it without the multiplexer. (This can, of course, always be done externally; but an internal termination would be tidier.)

Appendix

Active Repeater Board Schematic

Connector pin numbers are for channel 0. Repeats 12 times per board. See tables below for connector pins for other channels. Tentative values for parts given where we have a reasonable guess.



Board size is 3″ on the sides with input and output connections, 2″ in the other direction.

Analog Repeater Board Input

Shield 0	1	2	Shield 0
+Sig 0	3	4	-Sig 0
Shield 1	5	6	Shield 1
+Sig 1	7	8	-Sig 1
Shield 2	9	10	Shield 2
+Sig 2	11	12	-Sig 2
Shield 3	13	14	Shield 3
+Sig 3	15	16	-Sig 3
Shield 4	17	18	Shield 4
+Sig 4	19	20	-Sig 4
Shield 5	21	22	Shield 5
+Sig 5	23	24	-Sig 5
Shield 5	25	26	Shield 5
+Sig 6	27	28	-Sig 6
Shield 6	29	30	Shield 6
+Sig 7	31	32	-Sig 7
Shield 7	33	34	Shield 7
+Sig 8	35	36	-Sig 8
Shield 8	37	38	Shield 8
+Sig 9	39	40	-Sig 9
Shield 9	41	42	Shield 9
+Sig 10	43	44	-Sig 10
Shield 10	45	46	Shield 10
+Sig 11	47	48	-Sig 11
Shield 11	49	50	Shield 11

Analog Repeater Board Output

+5V (in)	1	2	Gnd
Out 0	3	4	Gnd
+5V (in)	5	6	Gnd
Out 1	7	8	Gnd
+5V (in)	9	10	Gnd
Out 2	11	12	Gnd
+5V (in)	13	14	Gnd
Out 3	15	16	Gnd
+5V (in)	17	18	Gnd
Out 4	19	20	Gnd
+5V (in)	21	22	Gnd
Out 5	23	24	Gnd
-5V (in)	25	26	Gnd
Out 6	27	28	Gnd
-5V (in)	29	30	Gnd
Out 7	31	32	Gnd
-5V (in)	33	34	Gnd
Out 8	35	36	Gnd
-5V (in)	37	38	Gnd
Out 9	39	40	Gnd
-5V (in)	41	42	Gnd
Out 10	43	44	Gnd
-5V (in)	45	46	Gnd
Out 11	47	48	Gnd
-5V (in)	49	50	Gnd