P1

VME_P1(159:0)

BGIN(3:0)

BGOUT(3:0)

BR(3:0)

VME_Controls(17:0)

GA*(4:0)

IRQ(7:1)

AM(5:0)

Address(23:1)

Data(15:0)

-12V

+5V_STDBY

+12V

+5V

VCC

TM0	Z1	129
ground	Z2	130
TM1	Z3	131
ground	Z4	132
TM2	Z5	133
ground	Z6	134
TM3	Z7	135
ground	Z8	136
TM4	Z9	137
ground	Z10	138
RTRY*	Z11	139
ground	Z12	140
ReservedBus0	Z13	141
ground	Z14	142
ReservedBus1	Z15	143
ground	Z16	144
ReservedBus2	Z17	145
ground	Z18	146
ReservedBus3	Z19	147
ground	Z20	148
ReservedBus4	Z21	149
ground	Z22	150
ReservedBus5	Z23	151
ground	Z24	152
ReservedBus6	Z25	153
ground	Z26	154
ReservedBus7	Z27	155
ground	Z28	156
SBB	Z29	157
ground	Z30	158
SBA	Z31	159
ground	Z32	160

D0	A1	1
D1	A2	2
D2	A3	3
D3	A4	4
D4	A5	5
D5	A6	6
D6	A7	7
D7	A8	8
ground	A9	9
SYSCLK	A10	10
ground	A11	11
DS1*	A12	12
DS0*	A13	13
WRITE*	A14	14
ground	A15	15
DTACK*	A16	16
ground	A17	17
AS*	A18	18
ground	A19	19
IACK*	A20	20
IACKIN*	A21	21
IACKOUT*	A22	22
AM4	A23	23
A7	A24	24
A6	A25	25
A5	A26	26
A4	A27	27
A3	A28	28
A2	A29	29
A1	A30	30
-12V	A31	31
+5V	A32	32

BBSY*	B1	33
BCLR*	B2	34
ACFAIL*	B3	35
BG0IN*	B4	36
BG0OUT*	B5	37
BG1IN*	B6	38
BG1OUT*	B7	39
BG2IN*	B8	40
BG2OUT*	B9	41
BG3IN*	B10	42
BG3OUT*	B11	43
BR0*	B12	44
BR1*	B13	45
BR2*	B14	46
BR3*	B15	47
AM0	B16	48
AM1	B17	49
AM2	B18	50
AM3	B19	51
ground	B20	52
SERCLK	B21	53
SERDAT*	B22	54
ground	B23	55
IRQ7*	B24	56
IRQ6*	B25	57
IRQ5*	B26	58
IRQ4*	B27	59
IRQ3*	B28	60
IRQ2*	B29	61
IRQ1*	B30	62
+5V_STDBY	B31	63
+5V	B32	64

D8	C1	65
D9	C2	66
D10	C3	67
D11	C4	68
D12	C5	69
D13	C6	70
D14	C7	71
D15	C8	72
ground	C9	73
SYSFAIL*	C10	74
BERR*	C11	75
SYSRESET*	C12	76
LWORD*	C13	77
AM5	C14	78
A23	C15	79
A22	C16	80
A21	C17	81
A20	C18	82
A19	C19	83
A18	C20	84
A17	C21	85
A16	C22	86
A15	C23	87
A14	C24	88
A13	C25	89
A12	C26	90
A11	C27	91
A10	C28	92
A9	C29	93
A8	C30	94
+12V	C31	95
+5V	C32	96

VPC	D1	97
ground	D2	98
+V1	D3	99
+V2	D4	100
ReservedU0	D5	101
-V1	D6	102
-V2	D7	103
ReservedU1	D8	104
GAP*	D9	105
GA0*	D10	106
GA1*	D11	107
+3.3V1	D12	108
GA2*	D13	109
+3.3V2	D14	110
GA3*	D15	111
+3.3V3	D16	112
GA4*	D17	113
+3.3V4	D18	114
ReservedBus8	D19	115
+3.3V5	D20	116
ReservedBus9	D21	117
+3.3V6	D22	118
ReservedBus10	D23	119
+3.3V7	D24	120
ReservedBus11	D25	121
+3.3V8	D26	122
LII*	D27	123
+3.3V9	D28	124
LIO*	D29	125
+3.3V10	D30	126
ground	D31	127
VPC	D32	128

To get +3.3V Power, the commented +3.3V Nets must be changed back to +3.3V.

Rows Z and D are in accordance with the VME64 Extensions standard. Note: the positioning of rows A, B and C should is still in accordance with the VME Standard.

DATE	REVISION DESCRIPTION
1998-12-11	Copied from PreFRED2 P1 -- MAB/WJA

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
VMEbus_P1

SHEET 5 OF 20
DATE 18 Nov 1996
DRWN JW

C-2421
REV A