The University of Chicago
The Enrico Fermi Institute
Electronics Development Group

SVX II Silicon Strip Detector Upgrade Project
Readout Electronics

The G-link Fiber Receiver Transition (GRT) Board

Design Specification

--PRELIMINARY--

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1 GENERAL INFORMATION

This document specifies the design of an HP G-link based fiber optic Receiver Transition board (referred to as the GRT from here on). A Gigabit-link (G-link) is a specialized high-speed chip set developed by Hewlett Packard corporation. It allows a “virtual ribbon cable” to be implemented: parallel data is serialized by the transmitter and sent over a high speed media (fiber or coax), received and de-serialized back into parallel data. All of this is accomplished with serial rates of up to 1.5Gbit/sec. This high rate lends the G-link to High Energy Physics applications.

The GRT will be part of the CDF SVX II Silicon Vertex Tracker (SVT) trigger and SVX DAQ systems. The goal of this document is to put forth an electrical and mechanical specification in sufficient detail to allow the board to be constructed. SVX system concepts mentioned here have been derived from references [1], [2], [3] and [4]. This is a preliminary document and the specifications developed here are likely to change.

1.1 System Introduction

(These paragraphs should briefly describe the system in which this component is used. This subsection should be identical for all components of a particular system. This section will be provided for you at a later date. It has not yet been written.)

1.2 Description Of Component & How It Fits Into The System

The GRT is a 9U transition board whose purpose is to receive serial optical data from the SVXII front end and parallelize it into TTL compatible levels for input to the SVT trigger and SVX DAQ systems. Specifically, the signals are accepted by the Hit Finder and VRB boards of the two systems, respectively. The GRT will reside in the rear of a standard CDF VME DAQ upgrade crate. It passes its signals through the J3 connector at the rear of the crate to a Hit Finder or VRB module residing in the front of the crate.

The Hit Finder, along with the VME Readout Buffer (VRB), receive hit data from the SVXII front end. This data is sent along fiber optic cables from the Fiber Interface Board (FIB) located in the collision hall. The FIB’s optical signals are sent first to an optical distribution box where the signals are split (with minimal loss) for transmission to the Hit Finder and VRB. The information passed along the optical fibers contain of *streams* of hit data which consist of address (position) and ADC value (magnitude) of hit silicon strips along with some housekeeping data. One optical cable will contain 2.5 streams (with the link operating in 20 bit mode). Each FIB contains 4 optical data ports. The entire SVX detector requires 36 FIBs to read out all data channels. Therefore, with each GRT containing 4 receivers it follows that 36 GRTs each will be needed to fully instrument the SVT and SVX DAQ systems.

1.3 List Of Component Requirements

-Receive a serial optical data stream and convert it into parallel data

-Contain four G-links per board

-Optical data rate ≈1.3GBit/s per channel

-Frame (parallel) data clocked out at 26MHz per channel

-G-link channels runs in either 16 or 20 bit mode (jumper selectable)

-G-link devices operate in unidirectional, simplex mode 2 (clock derived from input signal with fill frames sent to hold lock)

-Outputs (control and data) are single ended TTL (except clock, which is differential)

-9U Height

-Data and Control signals routed on J3 connector (using G-link/Taxi pinout)

-Power routed on J0 connector

-Reserve 32 pins on row B of J3 connector for VRB control bus

-Contain an identifier pin to distinguish between G-link and TAXI versions

-Adhere to VME-P requirements for transition cards

- +5V, operation

2 THEORY OF OPERATION AND OPERATING MODES

2.1 Basic Features & Operation

The function of the GRT is to receive data transmitted serially by a laser diode on the FIB and convert this optical signal into parallel data. This is accomplished in two stages. First, the optical signal in received and converted into a serial stream of switching voltages. Secondly, the serial voltage levels are then converted into parallel data. The first part is accomplished using an optical receiver. The optical receiver contains a photodiode and transimpedance amplifier along with support circuitry to convert the light pulses into serial voltages. The optical receiver that will be used for the GRT is the Finisar FRM-8510 built by Finisar Corporation [5]. This device is completely self contained with an ST connector to accept an optical fiber and ECL compatible serial outputs.

The outputs of the FRM-8510 pass into a Hewlett-Packard HDMP-1024 G-link receiver chip [6]. This chip contains all of the necessary clocking and demultiplexing circuitry required to convert high-speed serial data into parallel data words. The G-link can roughly be thought of as a special high speed UART. The transmitting end (FIB) contains another G-link (the HDMP-1022 transmitter). Together the two devices implement a simplex serial data link. The serial data is sent in frames. There are three types of frames: data, control and fill. The FIB to SVT/VRB link is unidirectional and operates in simplex mode 2 as specified by HP. In this mode, a periodic sync pulse is injected at the transmitter via the Tx G-link's ED pin. This forces a Fill Frame to be sent. The receiver's PLL uses the master transition in the fill frame to establish frequency and phase lock. When this occurs, the receiver is ready to accept data.

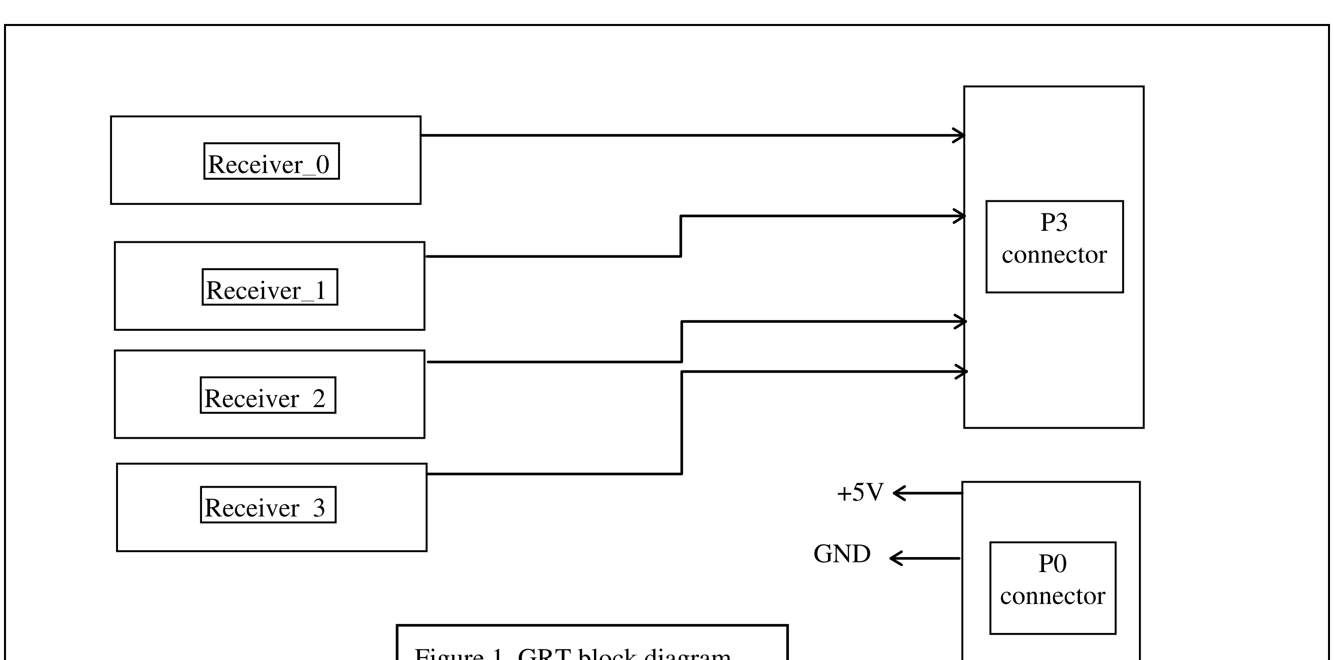

Figure 1. GRT block diagram.

Figure 1 shows a block diagram of the GRT. The overall architecture of the GRT is straightforward. It contains four individual receivers. The receivers are discussed further below. The outputs of the receivers are connected to the P3 connector. Each receiver attaches 25 signals to this connector. The P0 connector is used to bring power in the GRT.

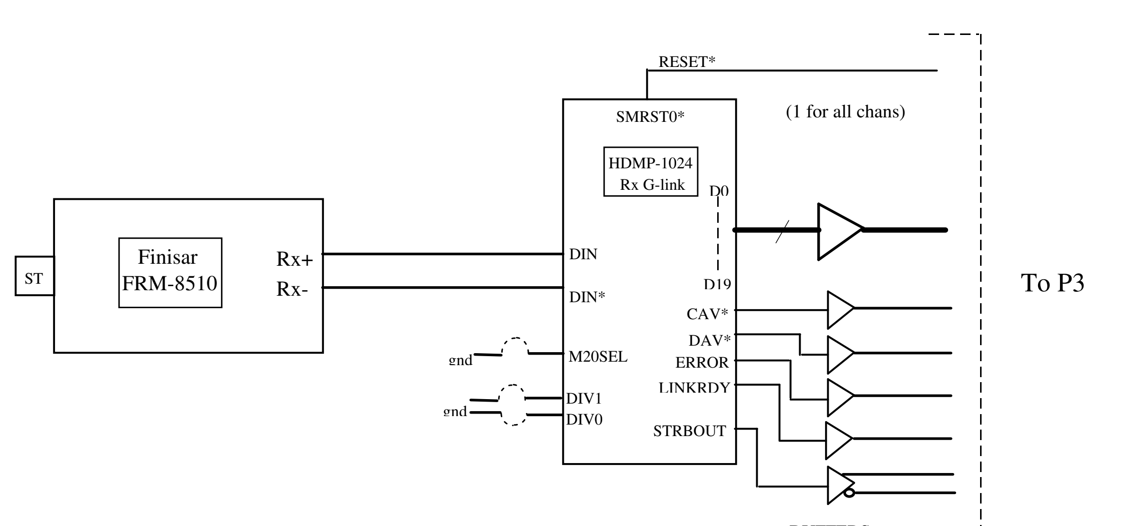

Figure 2. Single GRT Receiver Channel

Each receiver contains a Finisar FRM-8510 optical receiver and HP HDMP-1024 G-link receiver pair.. A block diagram of one receiver is shown in figure 2. The FRM-8510 has an ST connector to accept type 65/125 or 50/125 multimode fiber line. It receives 850nm optical pulses and outputs the serial ECL voltages to the G-link. The 1024 is configured to run in 20 bit mode for the Hit Finder/VRB. A jumper is provided to select 16 bit mode for other applications. For 20 bit mode, this gives a data frame length of 24 bits (20 data plus 4 control). Two additional jumpers (DIV1, DIV0) select the frequency range to the 1024’s internal PLL. These can be used to change the data rate of the link. This can be useful during hardware debug.

Data bits D0-D19 are passed out along with 5 control signals: CAV*, DAV*, STRBOUT, ERROR and LINKRDY*. Note that STRBOUT is brought out differentially. This is the recovered frame clock. It runs at 53MHz and to insure proper operation, this signal is made differential. These signals are discussed further in section 4. A reset input, RESET*, is used to reset the 1024’s internal state machine. A reset is generated at power up to initialize the device and also when an error occurs. This signal is generated by the Hit Finder or VRB module.

The data and control signals on the 1024 are at TTL levels. These signals are applied to a set of buffers followed by 33 ohm series terminator resistors before being passed into the J3 connector. One 74FCT162244CT (propagation delay range 1.5ns to 4.1 ns) and one 74FCT2541CT (propagation delay range from 1.5ns to 4.3ns) are used for D0-D19, CAV*, DAV*, ERROR and LINKRDY*. The STRBOUT clock differential pair is created with one 74AS86 (exclusive OR gates). This device has a propagation delay of 3.6nS.

The unbuffered RESET* input is distributed to all four 1024 devices.

A single set of jumpers are used for the MO20SEL, DIV1, and DIV0 lines, with lines running to all four receivers.

2.2 Diagnostic Features

Since the GRT does not need to possess a VMEbus interface, “in system diagnostics” cannot be accomplished using the local crate processor. However, the GRT will be tested prior to installation. In addition, the G-link devices themselves incorporate an error checking mechanism.

2.2.1 Production Testing

For production testing, it has been decided to use the Bit Error Rate Tester (BERT) system developed by the FNAL CD/ESE group. This system allows the GRT to be tested in a complete loop. It is described in [7]. Only one channel at a time can be tested but this is sufficient to insure the board is operating prior to installation.

2.2.2 In-Situ Error Detection

The G-link chip has internal error checking resources so that when lock is lost an ERROR signal is generated. Lock can be lost by failure of some component in the link, such as severing of the fiber optic cable, power failure at the Tx end, etc. The decision of how to handle this error signal is considered in the Hit Finder and VRB designs.

For the Hit Finder design, an additional form of error checking is being considered. This scheme involves reading out the SVX Chip ID numbers present in the data stream and comparing them with a lookup table of expected values. If an ID number does not match, this can be indicative of a soft error occurring in the link. While this method may not be an exhaustive test, it does provide an additional avenue for error checking.

3 EMBEDDED & DIAGNOSTIC/DEVELOPMENT SOFTWARE

(This section is not written until later in the development phase, not too much later though.)

4 INTERFACE SPECIFICATIONS

The GRT uses a total of 6 connectors (4 ST, P3 & P0) to input and output the necessary signals and power. These are discussed below.

4.1 VMEbus Interface

The GRT does not implement the VMEbus. Its main purpose is to convert signals from one media and format to another. Therefore the P1 connector will not be placed on the board.

4.2 Front Panel I/O, Test & Monitoring

The front panel of the GRT will contain four ST connectors for fiber input to the Finisar devices. Figure 3 shows the outline.

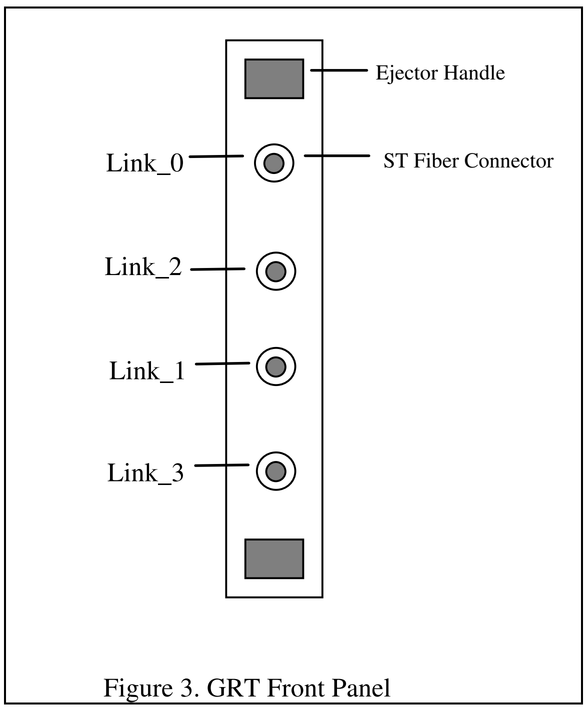

Figure 3. GRT Front Panel

4.2.1 First Connector

The ST connectors are integrated into the Finisar devices. The ST contains keying to insure proper alignment of the fiber. The arrangement of the receiver channels should be noted. Link_n corresponds to the grouping of signals on the P3 connector. The receiver inputs were arranged this way to make trace routing easier.

4.3 Rear Auxiliary Connector Interface

The P3 connector is used to pass all of the signals to the Hit Finder. Power will be brought in on P0. The pinouts of each P3 and P0 are listed below. The pin designations for P0 are taken from table 2 of [8].

4.3.1 Connector Pin Configurations

Table 1 lists the pinout of the P3 connector. P3 is a 235 pin (5 row x 47 pin) hard metric plug with 2 mm pin spacing. It does not contain any alignment guides. Similarly, P0 is also a 2mm hard metric plug with 133 pins (7 row x 19 pin). On both of the connectors, row F is used to provide extra ground. Physically, row F is a layer of metal on the outside of the connector housing.

PIN NUMBER	ROW A	ROW B	ROW C	ROW D	ROW E	ROW F
1	L0_D0	GND	rsrv	GND	L2_D0	GND
2	L0_D1	L0_D2	rsrv	L2_D2	L2_D1	GND
3	GND	L0_D3	rsrv	L2_D3	GND	GND
4	L0_D5	L0_D4	rsrv	L2_D4	L2_D5	GND
5	L0_D6	GND	rsrv	GND	L2_D6	GND
6	L0_D7	L0_D8	rsrv	L2_D8	L2_D7	GND
7	GND	L0_D9	rsrv	L2_D9	GND	GND
8	L0_D11	L0_D10	rsrv	L2_D10	L2_D11	GND
9	L0_D12	GND	rsrv	GND	L2_D12	GND
10	L0_D13	L0_D14	rsrv	L2_D14	L2_D13	GND
11	GND	L0_D15	rsrv	L2_D15	GND	GND
12	L0_D16	L0_D16	rsrv	L2_D16	L2_D16	GND
13	L0_D17	GND	rsrv	GND	L2_D17	GND
14	L0_D17	L0_D18	rsrv	L2_D18	L2_D17	GND
15	GND	L0_D18	rsrv	L2_D18	GND	GND
16	L0_D19	L0_D19	rsrv	L2_D19	L2_D19	GND
17	L0_CAV*	GND	rsrv	GND	L2_CAV*	GND
18	L0_DAV*	L0_LNKRDY*	rsrv	L2_LNKRDY*	L2_DAV*	GND
19	GND	L0_LNKRDY*	rsrv	L2_LNKRDY*	GND	GND
20	L0_STRBOUT	GND	rsrv	GND	L2_STRBOUT	GND
21	L0_STRBOUT*	L0_ERROR	rsrv	L2_ERROR	L2_STRBOUT*	GND
22	GND	L0_ERROR	rsrv	L2_ERROR	GND	GND
23	(GND)	GND	rsrv	GND	(GND)	GND
24	(GND)	(GND)	rsrv	(GND)	(GND)	GND
25	GND	(GND)	rsrv	(GND)	GND	GND
26	L1_CAV*	GND	rsrv	GND	L3_CAV*	GND
27	L1_DAV*	L1_LNKRDY*	rsrv	L3_LNKRDY*	L3_DAV*	GND
28	GND	L1_LNKRDY*	rsrv	L3_LNKRDY*	GND	GND
29	L1_STRBOUT	GND	rsrv	GND	L3_STRBOUT	GND
30	L1_STRBOUT*	L1_ERROR	rsrv	L3_ERROR	L3_STRBOUT*	GND
31	GND	L1_ERROR	rsrv	L3_ERROR	GND	GND
32	L1_D0	GND	rsrv	GND	L3_D0	GND
33	L1_D1	L1_D2	n/c	L3_D2	L3_D1	GND
34	GND	L1_D3	n/c	L3_D3	GND	GND
35	L1_D5	L1_D4	n/c	L3_D4	L3_D5	GND
36	L1_D6	GND	(GND)	GND	L3_D6	GND
37	L1_D7	L1_D8	(GND)	L3_D8	L3_D7	GND
38	GND	L1_D9	(GND)	L3_D9	GND	GND
39	L1_D11	L1_D10	(GND)	L3_D10	L3_D11	GND
40	L1_D12	GND	(GND)	GND	L3_D12	GND
41	L1_D13	L1_D14	n/c	L3_D14	L3_D13	GND
42	GND	L1_D15	n/c	L3_D15	GND	GND
43	L1_D16	L1_D16	n/c	L3_D16	L3_D16	GND
44	L1_D17	GND	n/c	GND	L3_D17	GND
45	L1_D17	L1_D18	n/c	L3_D18	L3_D17	GND
46	GND	L1_D18	RESET*	L3_D18	GND	GND
47	L1_D19	L1_D19	MODID	L3_D19	L3_D19	GND

Table 1: J3 Connector

PIN NUMBER	**ROW A**	**ROW B**	**ROW C**	**ROW D**	**ROW E**	**ROW F**
1	+5V	+5V	+5V	+5V	+5V	GND
2	rsrvd	rsrvd	+5V	rsrvd	rsrvd	GND
3	rsrvd	rsrvd	rsrvd	rsrvd	rsrvd	GND
4	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
5	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
6	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
7	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
8	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
9	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
10	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
11	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
12	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
13	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
14	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
15	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
16	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
17	unused	USER I/O	USER I/O	USER I/O	USER I/O	GND
18	rsrvd	USER I/O	USER I/O	USER I/O	USER I/O	GND
19	rsrvd	USER I/O	USER I/O	USER I/O	USER I/O	GND

Table 2: J0 Connector

4.3.2 Signal Descriptions

4.3.2.1 P3 Signals

Ln_$D_{0\text{-}19}$ Output. Data signals from G-links; TTL. Qualified with STRBOUT.

Ln_DAV* Output Status Signal: Indicates $D_{0\text{-}19}$ have valid data frame available; TTL.

Ln_CAV* Output Status Signal: Indicates $D_{0\text{-}19}$ contain valid control frame; TTL.

Ln_LINKRDY* Output Status Signal: Indicates G-link initialized and ready; TTL. Qualifies DAV* and CAV*

Ln_ERROR Output Status Signal: Indicates invalid frame has been received; TTL.

Ln_STRBOUT, Ln_STRBOUT* Output Clock Signal: Recovered frame rate clock. All above signals should be latched on rising edge. Differential TTL.

RESET* Input Control Signal: Resets all 4 G-links; TTL.

MODID Identifier. Indicates transition board is G-link (nc) or TAXI (Gnd).

The first 32 pins of row B are reserved for a special control bus used by the VRB.

Note that the GNDs indicated in parenthesis become signals in the TAXI transition module. Also, several data signals, $D_{16\text{-}19}$, are placed on two pins. This was done to also accommodate the TAXI signal requirements. On the GRT, one or both of these pins may be used.

4.3.2.2P0 Signals

P0 is used to power the GRT. With the GRT drawing approximately 4A(section 5.3) six 5V pins are sufficient. The row F pins are used for ground.

5 ELECTRICAL & MECHANICAL SPECIFICATIONS

5.1 Packaging & Physical Size

- Height: 9U
- Depth: 120mm

5.2 PC Board Construction

- 8 Layers
- 0.093 inch thickness
- Controlled Impedance Traces ($Z_0 = 124\Omega$) microstrip and embedded microstrip
- 4 signal layers, 4 power layers

5.3 Power Requirements

- Voltage= +5.0 V; Current= 4A; Power=20W.

5.4 Cooling Requirements

5.5 Board Layout

Figure 4 shows a screen capture of the GRT PCB from the CAD layout program. The P0 and P3 connectors are clearly shown. The Finisar devices and the G-links are indicated also. (U1_0,…,U1_3 and U2_0,…,U2_3). Note the close placement of the components in each of the receiver channels. The channels are placed close to each other to minimize the length of traces running to the P3 connector.

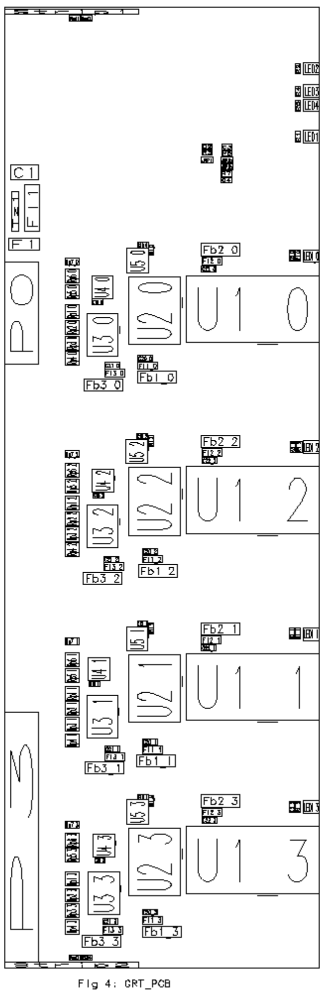

Fig. 4: GRT_PCB

6 SAFETY FEATURES & QUALITY ASSURANCE PROCEDURES

6.1 Module Fusing & Transient Suppression

Printed circuit board layouts include fusing and transient suppression for all incoming voltages. Fuses and transient suppression devices are placed as close as possible to the voltage entry point on the board. Fuses are sized such that the board is protected against a power short on the board. A single fuse per input voltage is used.

6.2 Other Safety & Quality Assurance Subsections

7 REFERENCES

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A APPENDICES

A1 List Of Component Documentation

A2 Schematics

A3 Parts List

A4 Additional Appendices