DRAFT
Version 0.2
July 1, 1997

Preliminary Component Specification of the SVT Hit Finder Board

J. Berryhill, R. Culbertson, H. Frisch, M. Shochet, P. Wilson

with the SVT and SVX-II Groups

University of Chicago

Abstract

The current components of the Hit Finder board are described. The inputs, outputs, and the function of each of its components are presented.

1 Introduction

The Hit Finder boards are the front line processors for the Level 2 SVT (Silicon Vertex Tracker) trigger system. Upon every Level 1 Accept, the SVX II detector is read out, and its optical output is split, with one of the streams directed to the GRT (G-link Receiver Transition) Card, which is a front panel connector to a Hit Finder board. The Hit Finder board interprets the SVX II readout (a series of channel number– ADC byte pairs), subtracts a programmable pedestal from each ADC byte, locates strings of consecutive channel numbers which have ADC above the pedestal, computes the ADC centroid for channels in this string, merges the centroid data from 10 different data streams, and passes the output to a merger board, the next stage in the SVT system.

2 Global input/output

The SVX II detector geometry determines the organization of optical readout lines and hence the Hit Finder input as well. The SVX II detector readout is partitioned into 6 logical barrels, each of which has 5 layers of silicon, each layer of which has 12 separate wedges, so that there are 360 separate data streams in all. A single Hit Finder board accepts the input of 1 wedge of all 5 layers of 2 logical barrels, so that each board accepts 10 separate data streams and the entire system requires 36 Hit Finder boards in all.

Each data stream is 8 bits wide. The GRT converts the optical fiber data to TTL via G-links running in 20 bit mode, so each G-link passes 2.5 data streams. Each 20 bit G-link data stream is also accompanied by 5 bits of control signals generated by the GRT:

- CAV*. Valid control frame.
- DAV*. Valid data frame available.

- STRBOUT. 53 MHz clock.
- ERROR. Invalid frame has been received.
- LINKRDY. G-link initialized and ready.

In order to accommodate 10 data streams, each GRT card has 4 G-links. This yields $(20+5) \times 4 = 100$ input lines coming through the P3 connector on the Hit Finder board.

The VME interface requires a 32-bit data bus, a 32-bit address bus, and a data strobe line. The particulars of the VME address map is given in [15].

The Hit Finder board output is a single 25-bit bus which is a sequence of cluster centroids.

The protocol is the standard SVT internal protocol [8], which is the official document. We briefly summarize it here.

The transfer is by 25 bits (50 pins) of LVDS. The source initiates the transfer of data, each data word is indicated by bit 23, the clock or data strobe (DS). The receiver module will be filling a FIFO with the data.

Bit 24 is almost full (AF) and is set high by the receiving board when its FIFO is almost full. When this bit is asserted, the source stops the transfer until the bit is cleared. Since almost full is signaled significantly before the receiver is actually full, the source is allowed many clock cycles to respond. Bit 21 is End Packet (EP) and is used to indicate the end of a logical group of data words. Bit 22 is called End Event (EE) and indicates that this is the last word being sent for this event. An EE must be sent for every event, whether or not and data words were sent.

pin	use	pin	use
1	centroid lsb_	2	centroid lsb
3	centroid_	4	centroid
	⋮		
29	centroid msb_	30	centroid msb
31	barrel lsb_	32	barrel lsb
33	barrel_	34	barrel
35	barrel msb_	36	barrel msb
37	layer lsb_	38	layer lsb
39	layer_	40	layer
41	layer msb_	42	layer msb
43	EP_	44	EP
45	EE_	46	EE
47	DS_	48	DS
49	AF_	50	AF

Table 1: Pinout for the hit finder to merger interface.

3 Data alignment FIFO's

Since 2.5 data streams are transmitted per G-link, 2 of the data streams on the Hit Finder board are split streams which come over 2 separate G-links with 2 different clocks (gstrbout).

Hit finder board (HF) input nodes		
Name	Origination	Function
gdata[19..0](0-3)	GRT	20-bit data bus
gcav(0-3)	GRT	valid control frame
gdav(0-3)	GRT	valid data frame available
gstrbout(0-3)	GRT	53 MHz clock
gerror(0-3)	GRT	invalid frame has been received
glinkrdy(0-3)	GRT	G-link initialized and ready
VMEdata[31..0]	VME	VME data bus
VMEaddress[31..0]	VME	VME address bus
VMEclk	VME	VME data strobe
Hit finder board (HF) output nodes		
Name	Destination	Function
VMEdata[31..0]	VME	VME data bus
hfdata[24..0]	Merger board	hit finder output bus

Table 2: A listing of input and output nodes of a hit finder board.

The separate clock lines are not necessarily synchronized and may be skewed by up to a full 53MHz clock cycle. Thus each half of the split stream is sent to a shallow FIFO, and the two FIFOs are read out by the same clock (presumably one of the gstrbout's), thereby aligning the two halves.

Data Alignment FIFO (DAFIFO) input nodes		
Name	Origination	Function
gdata[3..0]	GRT	4-bit split data stream
gstrbout	GRT	read request
gstrbout'	GRT	write request
Data Alignment FIFO (DAFIFO) output nodes		
Name	Destination	Function
adata[3..0]	DEMUX	4-bit split data stream
dempty	DEMUX	FIFO empty
dfull	DEMUX	FIFO full
dafull	DEMUX	FIFO above some almost full threshold

Table 3: A listing of input and output nodes of a data alignment FIFO.

4 Data demultiplexers

Each data stream is an alternating sequence of 8-bit words, where the first word has chip ID/channel number information, and the alternating word has chip status/ADC count information. The processor chip (see Processor) performs parallel synchronous operations at 26 MHz, half of the 53 MHz data stream input rate, so each (aligned) stream must be demultiplexed from one 8 bit stream into 2 8 bit streams. This operation can be performed before or after alignment. This operation can be done on a stream by stream (10 devices) or a G-link by G-link (4 devices) basis.

Data demultiplexer (DEMUX) input nodes		
Name	Origination	Function
gdata[19..0]	GRT	data
gstrbout	GRT	53 MHz clock
gdav	GRT	data valid from GRT
Data demultiplexer (DEMUX) output nodes		
Name	Destination	Function
dav	PREPROC	data valid bit to PREPROC
chan[7..0]	PREPROC	8-bit channel number to PREPROC
adc[7..0]	PREPROC	8-bit ADC count to PREPROC
hclock	PREPROC	26.5 MHz clock to PREPROC

Table 4: A listing of input and output nodes of a data demultiplexer.

5 Processors

All of the data stream interpretation, cluster finding, and cluster centroid computation are performed with Altera FLEX10K240R-50 EPLDs, one for each data stream (10 in all). The cluster finding logic consists of two stages: a preprocessing stage, where the SVX II readout is interpreted and valid ADC bytes undergo a programmable pedestal subtraction; and a cluster engine stage, where adjacent strips with ADC count above pedestal are grouped together, and the ADC-weigthed centroid of the group is computed. In addition, the processor chip contains buses and switches responsible for transferring data over a 16-bit VME data bus to the ISPY, PEDRAM, CRAM, and OFIFO, all of whose ports are connected to the processor chip.

5.1 Preprocessor

The preprocessor portion of the processor chip accepts two 8 bit streams of data from either the DEMUX devices or the ISPY buffers, using a 26.5 MHz clock line from the DEMUX device (hclock) or from a VME clock line (VMEclk). A bus line from VME (VMEcontrol) controls the data flow of the bidirectional ISPY connection lines (spychan, spyadc) as well as externally setting a state machine (ppstate) internal to the preprocessor.

The preprocessor interprets the data stream, in particular identifying the beginning of an event, the presence of chip ID bytes ($r-\phi$ or $r-z$), and the end of an event. Each $r-\phi$ chip ID increments a counter which determines the chip number corresponding to subsequent data. The first $r-z$ chip ID in a stream is identified and end of event is indicated at that time. Chip number is appended to the 7 bit channel number to give a 10 bit strip number (strip[9..0]). Strip number is input to an internal RAM (PEDRAM) containing ADC pedestals for that strip number. The pedestal is subtracted from the input

ADC and if the difference is greater than 0 the output (subadc) is sent along with the strip number to the engine logic.

Processor (HITMAN) input nodes		
Name	Origination	Function
dav	DEMUX	data valid bit from GRT
chan[7..0]	DEMUX	8-bit channel number from GRT
adc[7..0]	DEMUX	8-bit ADC count from GRT
hclock	DEMUX	26.5 MHz clock from GRT
VMEaddress[15..0]	VMEI	VME address bus
VMEclock	VMEI	clock from VME for ISPY input
testclock	BRAIN	test clock
brain[4..0]	BRAIN	5-bit control bus from the brain
Processor (HITMAN) output nodes		
Name	Destination	Function
spychan[7..0]	ISPY	8-bit channel number to ISPY
spyadc[7..0]	ISPY	8-bit ADC count to ISPY
cramadd[14..0]	CRAM	15-bit lookup RAM address
centroid[13..0]	OFIFO	14-bit cluster centroid coordinate
goodclus	OFIFO	cluster centroid valid
longclus	OFIFO	long cluster
outclk	OFIFO	26.5 MHz gated clock to OFIFO
Processor (HITMAN) bidirectional nodes		
Name	Destination	Function
VMEdata[15..0]	VMEI	VME data bus
spychan[7..0]	ISPY	8-bit channel number to ISPY
spyadc[7..0]	ISPY	8-bit ADC count to ISPY
cramdata[5..0]	CRAM	6-bit centroid offset from lookup RAM

Table 5: A listing of input and output nodes of a processor chip.

5.2 Cluster engine

The cluster engine accepts a sequence of strips and pedestal-subtracted ADCs at 26.5 MHz and outputs a 14-bit cluster centroid to an output FIFO (OFIFO). The engine logic identifies clusters through the comparison of consecutive strip numbers. Up to 6 adjacent strips are identified, the last strip in the cluster is tagged, each strip belonging to a long cluster (more than 3 adjacent strips) is tagged, and the ADCs from all strips in the cluster are summed.

5.3 VME bus tranceivers

In addition to data processing, the processor chip is responsible for VME communication with the ISPY, CRAM, PEDRAM, and OFIFO.

5.4 Operating modes

Listed below are the different operating modes of the processor chip.

- **Chip configuration.**
- **Read/write PEDRAM over VME.**
- **Read/write CRAM over VME.**
- **Read/write ISPY over VME.**
- **Writing to OFIFO from VME.**
- **Read/write adcthresh over VME.**
- **Read/write totadcthresh over VME.**
- **Initialization.**
- **Writing test data from ISPY.**
- **Normal data taking.**
- **SPY freeze cycle.**
  Read/write freezeaddress over VME.
  Read/write spystate over VME.
  Read ISPY over VME.

6 Input SPY buffers

An ISPY buffer is a RAM which is a continuously updated record of a data stream being input to a preprocessor. There exists one ISPY buffer for each data stream = 10 ISPY buffers in all. Each ISPY buffer stores 16-bit words consisting of the 8-bit channel number and 8-bit ADC count received by each preprocessor. During normal operation, the ISPY buffer reads the 16-bit data words at 26.5 MHz, with a clock signal from the preprocessor identical to the preprocessor's input clock (PREPROC:hclock). The address is generated by a counter inside the preprocessor which is clocked by the same signal. Once all addresses have been written to, the counter resets to zero and the ISPY buffer is over-written, so that it contains a history of processor chip input for the past N = (ISPY RAM depth) data words.

The ISPY can also be read to/written from by VME, which can communicate to the ISPY via buses within the processor chip. This allows for sampling of the ISPY contents for monitoring and debugging of the SVT system, as well as loading test data over VME which can subsequently be clocked back through the processor chip using a test clock signal.

The ISPY depth should be deep enough to accomodate several 100% occupancy events read out for a single data stream. Each data stream can be as many as 1300 16-bit words long, so the minimum depth for recording 10 100% occupancy events is about 16K. A 64K depth is used in current designs.

One such 64K X 16 bit RAM is a Motorola 64K X 18 fast SRAM (MCM67B618A). The SRAM is packaged in a 52 pin PLCC casing. The pins used are given in Table 6.

Input SPY buffer (ISPY) input nodes		
Name	Origination	Function
D0–D7	PREPROC:spychan[7..0]	8-bit channel number
D8–D15	PREPROC:spyadc[7..0]	8-bit ADC count
K	PREPROC:spyclock	clock
A0-A15	PREPROC:spyaddress[15..0]	RAM input address
LW–UW	PREPROC:spywrite	lower 8/ upper 8 bit write enable
G	PREPROC:spywrite	output enable (initiates read cycle)
Input SPY buffer (ISPY) output nodes		
Name	Destination	Function
D0–D7	PREPROC:spychan[7..0]	8-bit channel number
D8–D15	PREPROC:spyadc[7..0]	8-bit ADC count

Table 6: A listing of input and output nodes of an input SPY buffer.

7 Cluster engine RAM

Each cluster engine requires a lookup RAM which receives as input 3 5-bit ADC counts and outputs a 6 bit centroid, which is added to the cluster center by the cluster engine to give the cluster centroid coordinate. The minimum memory required is $2^{3\times 5} \times 6 = 24.6$ kB.

During normal operation, the RAM is clocked and addressed by the processor chip and 6 bits of data are read back to the processor chip. The CRAM can also be written to/read from by VME, which can communicate to the CRAM via buses within the processor chip.

One such 32K X 6 bit RAM is a Motorola 32K X 9 fast SRAM (MCM62940B). The SRAM is packaged in a 44 pin PLCC casing. The pins used are given in Table 7.

Cluster engine RAM (CRAM) input nodes		
Name	Origination	Function
D0–D5	ENG:cramdata[5..0]	6-bit centroid offset
K	ENG:cramclock	clock
A0-A15	ENG:cramadd[14..0]	RAM input address
W	ENG:cramwrite	write enable
G	ENG:cramwrite	output enable (initiates read cycle)
Cluster engine RAM (CRAM) output nodes		
Name	Destination	Function
D0–D5	ENG:cramdata[5..0]	6-bit centroid offset

Table 7: A listing of input and output nodes of a cluster engine RAM.

8 Output FIFO's

Each cluster engine RAM outputs 16-bit data words to an output FIFO (OFIFO) at clock speeds up to 26.5 MHz, which subsequently writes 16-bit data words to the MOP at clock speeds up to 30 MHz. FIFO status signals (FIFO full, almost full, empty) are sent to the MOP.

The OFIFO depth should be deep enough to accomodate several 100% occupancy events read out for a single data stream. Each data stream can be as many as 1300 16-bit words long, so the minimum depth for recording 10 100% occupancy events is about 16K. A 16K depth is used in current designs.

One such FIFO is an Integrated Device Technology 16K X 18 CMOS Supersync FIFO (IDT72265). The FIFO is packaged in a 68 pin PGA case. The pins used are given in Table 8.

Output FIFO (OFIFO) input nodes		
Name	Origination	Function
D0–D15	ENG:outdata[15..0]	16-bit data stream
WCLK	ENG:outclock	write clock
RCLK	MOP	read clock
WEN	ENG:outwrite	write enable
REN	MOP	read enable
OE	MOP	output enable (tri-states output)
PRS	MOP	partial reset (initializes pointers)
MRS	MOP	master reset (initializes FIFO mode)
Output FIFO (OFIFO) output nodes		
Name	Destination	Function
Q0–Q15	MOP	16-bit data stream
EF	MOP	FIFO empty
FF	MOP	FIFO full
HF	MOP	FIFO half full

Table 8: A listing of input and output nodes of an output FIFO.

9 Merger and Output Processor

An EPLD must coordinate the readout of 10 output FIFOs from the 10 processors in order to merge them into a single readout stream at 30 MHz or less.

10 Coordinate transform RAM

The coordinate transform RAM The hit coordinates output by the hit finder board consists of 21-bit words. Each word should identify a unique 1/32 of a particular strip in SVX II. The particular coordinate system in which these hits take their 21-bit representation is currently

Merger and Output Processor (MOP) input nodes		
Name	Origination	Function
mopclock	heart	master clock for MOP
mopcontrol	brain	on/off switch
mbdata[15..0]	MOPBUS	16-bit data from one of the OFIFOs
ofull[9..0]	OFIFOs	OFIFO full
oempty[9..0]	OFIFOs	OFIFO empty
oafull[9..0]	OFIFOs	OFIFO almost full
HD	merger board	merger board not ready
Merger and Output Processor (MOP) output nodes		
Name	Destination	Function
mdata[24..0]	merger board	output bus of Hit Finder board
DS	merger board	strobe output bus
mread	MOPBUS	read request of OFIFO

Table 9: A listing of input and output nodes of the Merger and Output Processor .

unspecified, and even if it is specified, it could be subject to change over time (*e.g., local alignment corrections could be implemented).*

11 Output SPY buffers

The OSPY buffer is a continuously updated record of the output of the Hit Finder board. Conversely the OSPY can be loaded by VME and used as test data for the merger board.

Output SPY buffer (OSPY) input nodes		
Name	Origination	Function
ospydata[24..0]	MOP	output stream of MOP
ospyclock	MOP	buffer clock
ospymode	brain	read/write control line
Output SPY buffer (OSPY) output nodes		
Name	Destination	Function
ospydata[24..0]	MOP	test data to be sent to MOP

Table 10: A listing of input and output nodes of an output SPY buffer.

12 VME interface

Ha!

13 heart

The MOP needs a clock to run it at around 30 MHz.

14 brain

References

[1] *Kerry Woodbury Fiber Interface Board ESE-SVX-951010, Feburary 11, 1997.*

[2] *John Dusatko The G-link Fiber Receiver Transition (GRT) Board September 4, 1996. (To be updated.)*

[3] *SVT group, SVT Technical Design Report.*

[4] *VRB group, SAR to SVT Processor Interface Protocol (draft).*

[5] *Hsaio Ying Chao and Jaroslav Antos Occupancy Study for the SVXII CDF note 2386, Nov 21, 1994.*

[6] *Ray Culbertson Occupancy in SVXII December 12, 1995.*

[7] *P. Murat The New Plug and Occupancies in Run II CDF Silicon Tracker CDF note 3720, March, 1997.*

[8] *S. Belforte et al Specification of the XTRP, SVT, and Level 2 Interfaces October 15, 1996.*

[9] *SVT group, SVT I/O Data Format Specifications, internal note 54.*

[10] *SVT group, Hit Buffer Technical Specifications, internal note 36.*

[11] *SVT group, Hit Buffer Specification and Design, internal note 51.*

[12] *Yale group, Conceptual design of the Trigger System Interface for the Run II Upgrade., Yale Trigger Note 1.*

[13] *Theresa M. Shaw, Research Division, Specification for TRigger And Clock + Event Readout Module (TRACER)., draft.*

[14] *John Conway et al Numbering and Naming Convention for the SVX-II and ISL CDF note 4103, March 12, 1997.*

[15] *Ray Culbertson VME Address Map May 6, 1997.*