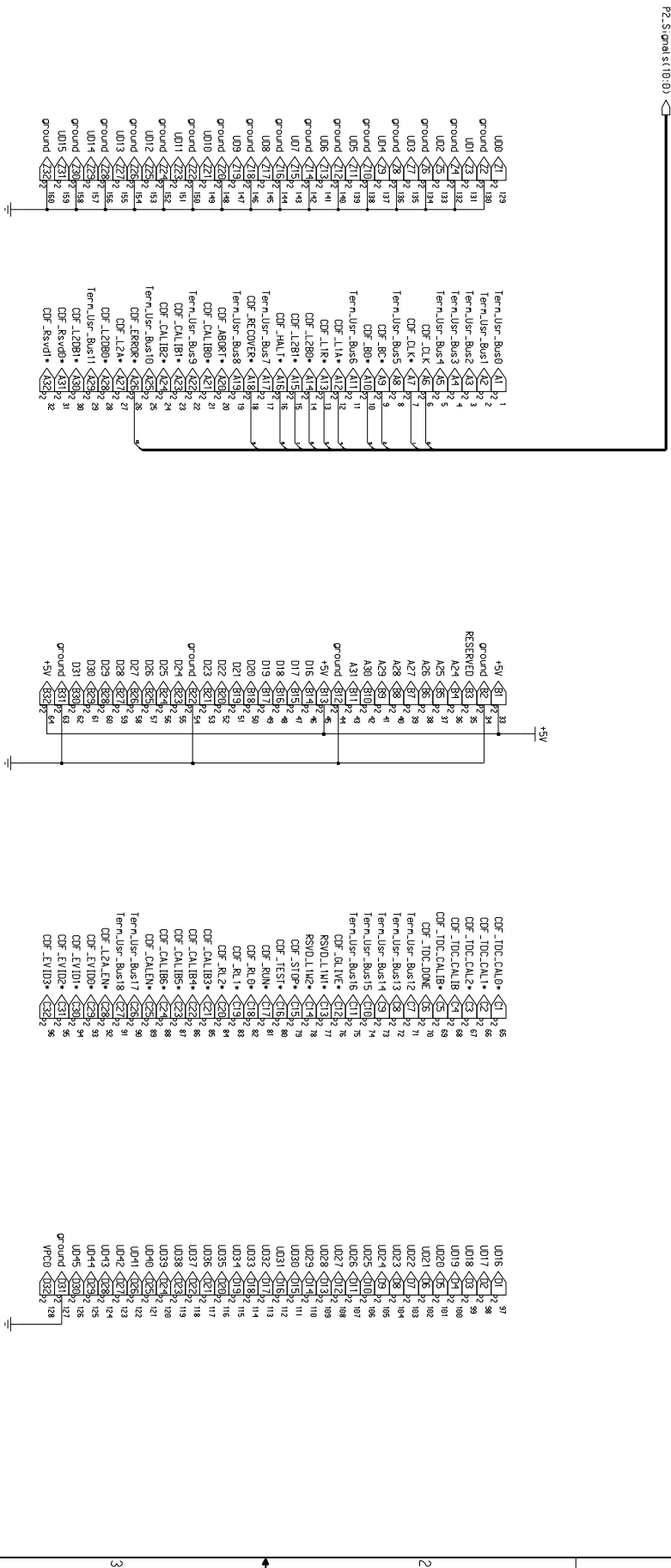


P2



Rows Z and D are in accordance with the VME64 Extensions standard. Note: the positioning of rows A, B and C should be in accordance with the VME Standard.

- a. All user-defined signals on P2 are totem-pole TTL excluding:
- b. 132ns Clock is differential PECL: CLK - CLK+
- c. ERROR+ is open collector TTL

DATE	REVISION DESCRIPTION	TITLE
16 Dec 93	Original design ... JF	UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP
31 Aug 94	Major 2 and 3 revisions to the VME64 Ext. Bus	
18 Nov 96	Final revision - final file	VMEbus_P2

SHEET 3 OF 10	C-2374
DATE 18 Nov 1996	REV B
DRMN JM	