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Hardware Design and Specification of the SVT Track Fitter

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Contents

1 Introduction

The SVT is one of the major components of the CDF trigger upgrade for RUN-II. It is designed to measure the impact parameter (d) of a track with a precision of 35 μm as well as improve on the measurement of the curvature (c) and the azimuthal angle (ϕ) of the track.

In the SVT system, the Track Fitter (TF) carries out the process of track fitting using the SVX-II hits and the curvature (c) and ϕ measurements from the XFT. The TF calculates the track parameters using a linear approximation in one SVX wedge (30 degrees in ϕ) [1]. The linear approximation allows us to calculate the track parameters, $\vec{p}$, from a simple scalar product of hits, $\vec{x}$:

$$p_i = \vec{f_i} \cdot \vec{x} + q_i, \tag{1}$$

where p_i is one of the track parameters. In this equation, $\vec{x}$ is a seven dimensional vector where x_0 to x_4 correspond to the hit positions in the five SVX layers, and x_5 and x_6 correspond to ϕ and c from the XFT, respectively. The SVT track can be reconstructed with good precision using the hits from only four SVX layers. Therefore, in Equation 1, we only use hits from four of the five SVX layers. The TF performs a track quality cut to select good track candidates. It calculates three track constraints (see reference [1]), each of which is also calculated with the linear approximation: $\chi_i = \vec{f_i} \cdot \vec{x} + q_i$. The total χ^2 is the sum of the squares of the three constraints: $\chi^2 = \chi_1^2 + \chi_2^2 + \chi_3^2$.

In summary, the main function of the TF is the calculation of the three track parameters (ϕ, d and c) and the χ^2 of the fit.

2 Hardware Design

2.1 Input and Output

The SVT system employs a uniform protocol ("SVT protocol" [2]) for data transfer. Each word is 25 bits wide. Twenty-three data bits and a clock are pushed from the source board to the destination board. In addition, there is one line driven by the destination to inform the source that the input FIFO is almost full.

2.1.1 Input

The input data to the TF are provided by the SVT Hit Buffer (HB) board. The data consist of the silicon hit information measured by the SVT Hit Finder (HF), the track parameters measured by the XFT, and the Associative Memory (AM) road identification number (ID) and sector ID (wedge number) from the AM pattern recognition. The contents of the input data are listed in Table 1. As shown in Table 1, the TF receives multiple SVT words per road. The minimum number of input words per road is seven: four SVXII hit words, two XFT words, and one AM road word. One of two XFT words is used for AM pattern recognition. The other is used by the TF and is identical to the original XFT output. When

Table 1: The input data to the TF from the HB. The format of the data structure is defined in reference [2]. In this table, "layer" is the SVX-II layer ID, "layer(XFT)" [:= 5] is the XFT layer ID in the SVT, "z" is the z barrel ID of the hit, "lc" is the bit that identifies a long cluster from the HF, and "PA" is the parity of the data [3].

<table>
<tr><td>bit</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>use</td><td>HD</td><td>DS</td><td>EE</td><td>EP</td><td colspan="21">data</td></tr>
<tr><td>wd1.1</td><td></td><td></td><td></td><td></td><td colspan="3">layer</td><td colspan="3">z</td><td>lc</td><td colspan="14">x_0</td></tr>
<tr><td>wd1.2</td><td></td><td></td><td></td><td></td><td colspan="3">layer</td><td colspan="3">z</td><td>lc</td><td colspan="14">x_1</td></tr>
<tr><td>wd1.3</td><td></td><td></td><td></td><td></td><td colspan="3">layer</td><td colspan="3">z</td><td>lc</td><td colspan="14">x'_1</td></tr>
<tr><td>wd1.x</td><td colspan="25">:</td></tr>
<tr><td>wd1.n</td><td></td><td></td><td></td><td></td><td colspan="3">layer(XFT)</td><td colspan="18">XFT information for the AM</td></tr>
<tr><td>wd1.(n+1)</td><td></td><td></td><td></td><td></td><td></td><td></td><td>sign</td><td colspan="6">c from the XFT</td><td colspan="12">ϕ from the XFT</td></tr>
<tr><td>wd1.(n+2)</td><td></td><td></td><td></td><td>1</td><td colspan="4">sector</td><td colspan="17">AM road ID</td></tr>
<tr><td>wd1.x</td><td colspan="25">:</td></tr>
<tr><td>end</td><td></td><td></td><td>1</td><td>1</td><td colspan="2">L2B</td><td colspan="10">error flags</td><td>PA</td><td colspan="8">Event Tag</td></tr>
</table>

there are more than one hit in a layer, the TF receives more than seven words per road, for example, the x'_1 hit in Table 1. The TF receives several roads per event when the AM system finds multiple track candidates. For an event in which no road is found, the TF receives only the end of event (EOE) word.

2.1.2 Output

The output of the TF consists of three track parameters, ϕ, d, and c. In addition, the TF sends the other information listed in Table 2. Some variables listed in Table 2 might not be important for the trigger decision, but are important for monitoring SVT performance both online and offline since only the TF output data are recorded in the CDF data stream. The output data from the TF are sent to the L2 interface board via an SVT Merger board. If no road passes the track quality cut or the event has no road, the TF only sends the EOE

Table 2: The SVT data sent to the L2 Interface board. The format of the data structure is defined in reference [2]. Each variable is defined in Table 3.

<table>
<tr><td>bit</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>use</td><td>HD</td><td>DS</td><td>EE</td><td>EP</td><td colspan="21">data</td></tr>
<tr><td>wd1.1</td><td></td><td></td><td></td><td></td><td>1</td><td></td><td colspan="6">z</td><td colspan="13">ϕ</td></tr>
<tr><td>wd1.2</td><td></td><td></td><td></td><td></td><td>0</td><td></td><td>sign</td><td colspan="8">c</td><td>sign</td><td colspan="9">d</td></tr>
<tr><td>wd1.3</td><td></td><td></td><td></td><td></td><td colspan="4">sector</td><td></td><td></td><td colspan="15">AM road ID</td></tr>
<tr><td>wd1.4</td><td></td><td></td><td></td><td></td><td></td><td colspan="10">x_1</td><td colspan="10">x_0</td></tr>
<tr><td>wd1.5</td><td></td><td></td><td></td><td></td><td></td><td colspan="10">x_3</td><td colspan="10">x_2</td></tr>
<tr><td>wd1.6</td><td></td><td></td><td></td><td></td><td colspan="11">χ^2</td><td colspan="10">x_4</td></tr>
<tr><td>wd1.7</td><td></td><td></td><td></td><td>1</td><td colspan="12">Track Fitter status</td><td colspan="9">Track Number</td></tr>
<tr><td>wd2.x</td><td colspan="25">:</td></tr>
<tr><td>end</td><td></td><td></td><td>1</td><td>1</td><td colspan="2">L2B</td><td colspan="10">error flags</td><td>PA</td><td colspan="8">Event Tag</td></tr>
</table>

word.

The details of each output parameter are listed in Table 3. The definitions of the error flags and the TF status word are found in Section 8. Although we send only the 8 LSB of

Table 3: The definition of the track parameters in the TF. The range and the least count of the track parameters depend on the fitting parameters, and they are adjustable.

Parameter	# bits	least count	range	Comments
ϕ	13	0.76 mrad	$< 2\pi(6.28)$	
z	6			three MS bits: z ID of the most outer hit, three LS bits: z ID of the most inner hit.
d	10	10 μm	$< 5,120$ μm	The MSB is the sign (1: negative).
c	9	$1.17 \times 10^{-3}\mathrm{m}^{-1}$	< 0.3 m^{-1}	The MSB is the sign (1: negative).
road ID	15		$\leq$32k	AM road ID
sector	4		$\leq$12	Sector ID
x_i	10	~ 4 μm	$\leq 1,024$ μm	8 LS bits of the hit position at the layer i; the second MSB is the long cluster bit; the MSB is the hit existence bit.
χ^2	11	1	$< 1,024$	The MSB is the overflow bit.
Track Number	9	22 mrad	$< 2\pi(6.28)$	The 9 MS bits of the XFT ϕ.
Track Fitter status	11			The MSB is OR of all errors. (see Section 8).
Event Tag	8			The bunch cross counter.
PA	1			the parity (see Section 6).
error flags	10			see Section 8.
L2B	2			L2 Buffer ID.

each SVX hit position, we can reconstruct the full hit position (14 bits) using the AM road ID as shown in Equation 2.

2.2 Conceptual Design

The main function of the TF is to execute the vector calculation of Equation 1. The $\vec{x}$ in Equation 1 is a seven dimensional vector with 14 bits of data for each SVX hit, 12 bits of XFT ϕ and 7 bits of XFT c. In order to obtain full resolution for the track parameters $\vec{f_i}$, we would have to perform 14-bit times 14-bit multiplication for seven products, and sum them to construct each track parameter. Such large calculations cannot be carried out with current technology for FPGAs (Field-Programmable Gate Array). Therefore, we use the following algorithm to reduce the load of the calculation in the FPGA. The range of $\vec{x}$ must be the size of the Super Strip (SS) in the AM road for that track candidate. If we define the lower edge of the SS in the AM road as $\vec{x}_0$, the relative coordinate of the hit in the SS is expressed as $\vec{d} = \vec{x} - \vec{x}_0$ (Note: x_0 is independent of curvature because track curvature is not used in the SS definition.). The range of $\vec{d}$ is the SS size, which is typically 500 μm or less. Thus $\vec{d}$ can be expressed with 8 bits with a least count of ~ 4 μm. With a linear approximation, we can express Equation 1 with the vectors $\vec{x_0}$ and $\vec{d}$ instead of $\vec{x}$:

$$p_i \quad = \quad \vec{f_i} \cdot (\vec{x}_0 + \vec{d}) + q_i,$$

$$p0_i + \delta p_i = (\vec{f}_i \cdot \vec{x}_0 + q_i) + \vec{f}_i \cdot \vec{d}, \qquad (2)$$

where

$$p0_i = \vec{f}_i \cdot \vec{x}_0 + q_i \qquad (3)$$

$$\delta p_i = \vec{f}_i \cdot \vec{d} \qquad (4)$$

In Equation 2, $p0_i$ is the track parameter for hits at the lower boundary of the SS in the AM road, which is calculable beforehand from the road definition. Thus in the TF, we do not have to calculate $p0_i$ event by event, but can use the pre-calculated values stored in a memory lookup table. Therefore, in the TF, we actually calculate δp_i in the FPGA and add the value of $p0_i$ from the memory lookup table. Currently available FPGAs, such as the ALTERA FLEX 10K100, make such calculations feasible. We use 8 bits for the contents of the $\vec{d}$. The 8 bits for the hit position allow a SS size up to 1,024 μm with a LSB of 4 μm. The concept is sketched in Figure 1.

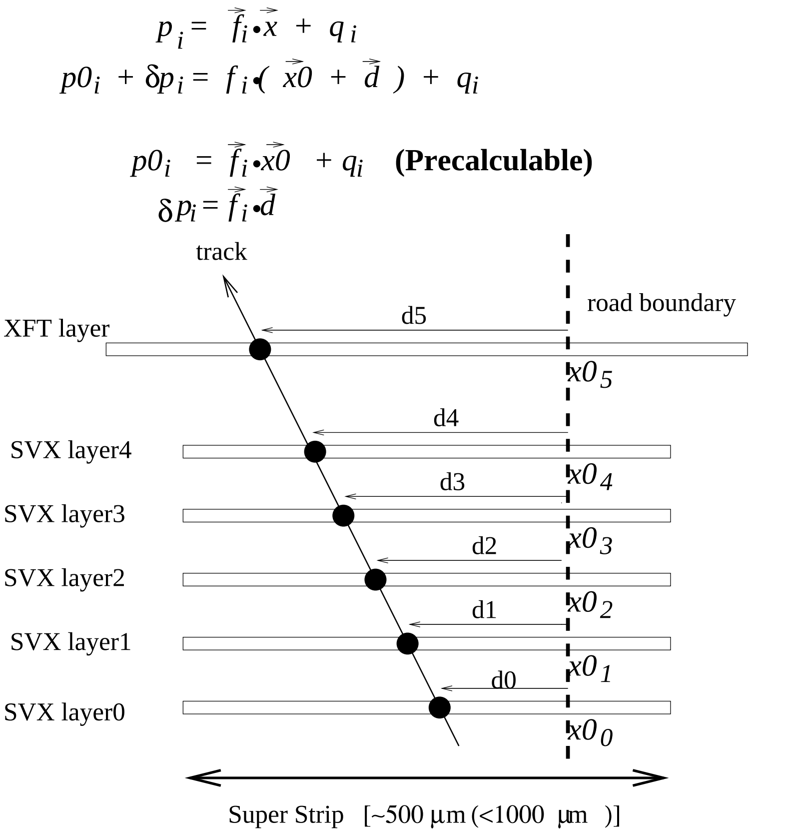


Figure 1: The concept of the fitting algorithm in the Track Fitter

In the fitting algorithm, we use a hit in each of four SVX layers even if there are hits in the road in all five SVX layers. The selection of the layers used in the fit is predetermined and stored in a memory lookup table based on both the presence of the hits and their quality as determined by the long-cluster bits produced by the HF.

If there are more than one hit in a layer, we must fit multiple combinations of hits. For example, when there are two hits in layer 0, x_0 and x'_0, and one hit in the other layers, we have two possible vectors, $\vec{x} = (x_0, x_1, x_2, x_3, x_5, x_6)$ and $\vec{x'} = (x'_0, x_1, x_2, x_3, x_5, x_6)$. The TF performs the calculation for all possible combinations of hits.

2.3 Overview of the TF Schematic and the Data Flow

The top diagram of the TF board schematic is shown in Figure 2. In Figure 2, the data come from the Front Panel, and flow through the FEP, the FITTER, and the OPP, and go out to the Front Panel. A simple diagram of the data flow is shown in Figure 3. Each block in the figures is introduced as follows.

FEP (Front End Processor) The data arriving from the HB are stored in the INPUT FIFO. The function of the FEP is to read the SVT data from the INPUT FIFO and form an internal TF word. This word contains all six hits (hits from five SVX layers and the XFT), with the two XFT track parameters packed into one hit. In addition, when there are multiple hits in a layer, the FEP creates TF words for all possible hit combinations.

TF_FIFO The TF_FIFO is a buffer to store the data between the FEP and the downstream fitting processor (FITTER). The TF_FIFO is in the FEP block in Figure 2. With a buffer between the FEP and the FITTER, the FITTER can run asynchronously from the FEP.

FITTER The function of the FITTER is to calculate the track parameters. The FITTER consists of one control component and 6 FIT components for the three track parameters and the three constraints.

OPP (OutPut Processor) The function of the OPP is to send the fitting results to the L2 interface board. The OPP collects the necessary information from the TF_FIFO and the FITTER, and packs it into the 7 SVT words shown in Table 2. In addition, the OPP takes care of the error handling in the TF, checks the track quality, and calculates the track χ^2. The OPP also records a part of the output data in FIFO's that are used to determine the beam position.

Front Panel The Front Panel is the interface between the TF board and other SVT boards. It follows the SVT protocol. In addition, the Front Panel also has an interface for configuring the FPGA chips.

In Section 3, we describe the function of each component in more detail.

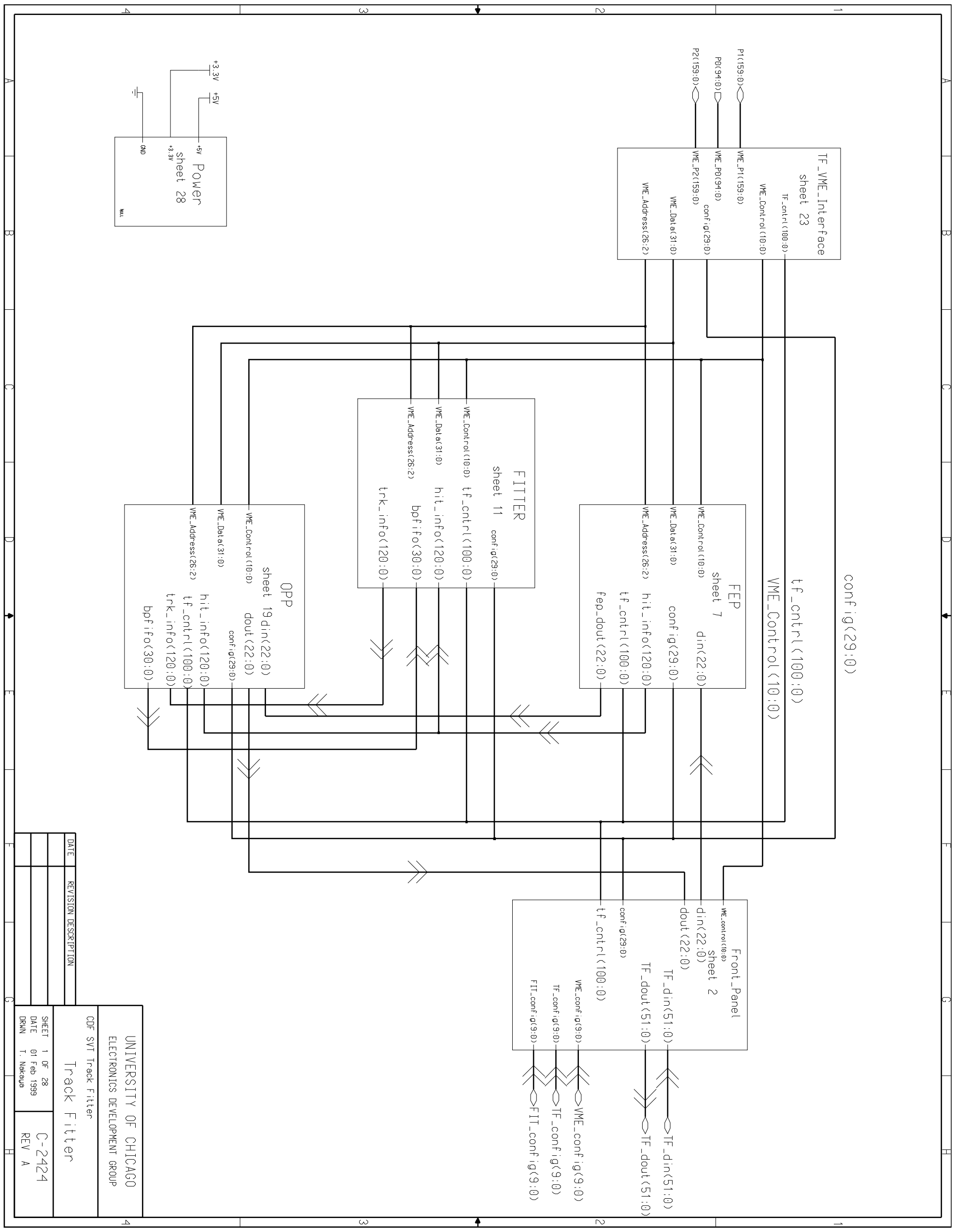


Figure 2: The top diagram of the TF board schematic. The din(22:0) are the incoming data from the INPUT_FIFO in the Front Panel. The FEP reconstructs the hit_info(120:0) from the incoming data, which are inputs to the FITTER and the OPP. The FITTER reconstructs the fit results, trk_info(120:0), which are sent to the OPP. Finally, the OPP sends the output data, dout(22:0), back to the Front Panel.

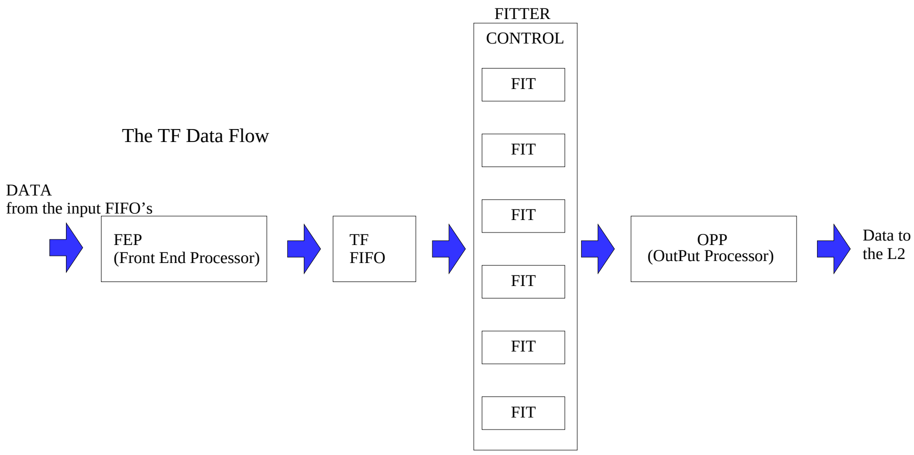


Figure 3: Diagram of the data flow in the Track Fitter.

2.4 Special SVT signals

All of the SVT boards have special signal lines that run across the VME P2 backplane. There are five signals including a spare line: SVT_INIT, SVT_ERROR, SVT_FREEZE, SVT_LOSTLOCK and SVT_SPARE. In the TF board, only SVT_INIT, SVT_ERROR, SVT_FREEZE and SVT_SPARE lines are used (connected). SVT_INIT is the signal to initialize the board. After receiving the signal, the board is ready to process data within 100 nsec. The SVT_ERROR signal is generated by the board if it detects an error condition as described in Table 10 in Section 8. SVT_FREEZE is used in the SPY buffer system as discussed in Section 4.2.

3 Front Panel

The top diagram of the Front Panel is shown in Figure 4. The Front Panel block consists of four components: DATAIN, DATAOUT, CONFIG and LED.

DATAIN The DATAIN block connects the input SVT connector to the INPUT FIFO. The SVT protocol is implemented on the TF board with National LVDS DS90C032A receivers and DS90C031A drivers, each of which has four channels. The input SVT data lines have 24 bits of incoming data and 1 bit of outgoing data (HOLD). We use six receivers and one driver in the DATAIN block. Downstream of the receivers, there are two CYPRESS CY7C4245 4k$\times$18 FIFO's to store the data. The almost-full signal from the FIFO's is fed back to the HOLD line through the LVDS driver. The method of FIFO control is described in reference [3].

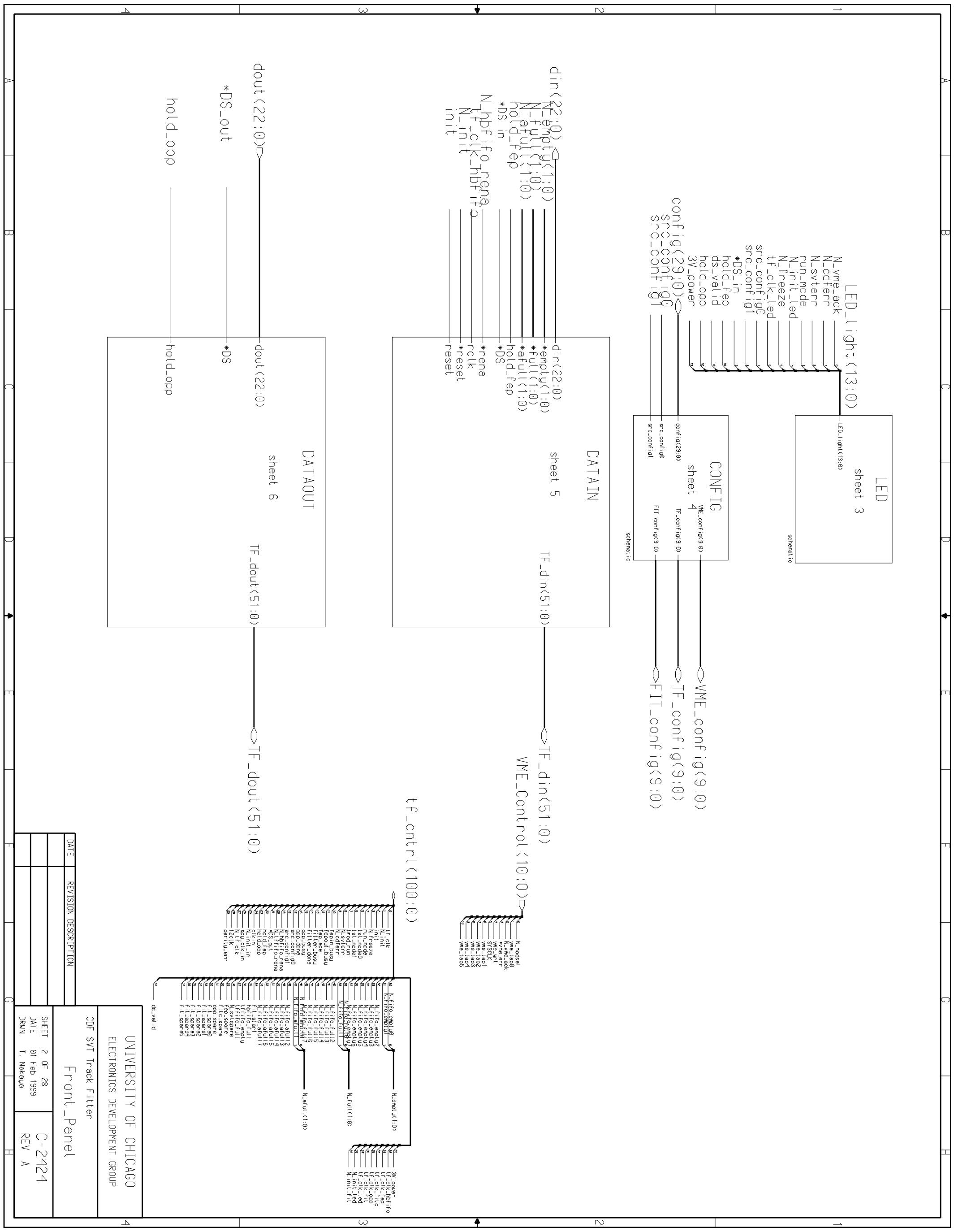


Figure 4: The top diagram of the Front Panel Schematic.

DATAOUT The DATAOUT block sends data to the output SVT connector. There are six LVDS drivers and one LVDS receiver, the inverse of DATAIN. As specified in the SVT protocol, the leading edge of the active low data strobe is adjusted to have T1 $= 10(> 6)$ nsec and T2 $= 15(> 10)$ nsec. (T1 and T2 are defined in Figure 2 in the reference [2].)

CONFIG The CONFIG block connects the bit blaster connector for configuring the FPGA chips. There are three connectors corresponding to the VME Interface chip (MAX7000), 6 FIT chips (FLEX10K), and 3 other control chips (FLEX10K). Since there are six big chips with the same program (FITTER/FIT), these six chips make one group. The other control chips (the FEP, the FITTER/CNTRL and the OPP) make another group. The CONFIG component includes an EPROM configuration device, EPC1, for the FLEX10K. We can select the source for the configuration to be either the EPC1 or the bit blaster connector on the front panel. One EPC1 has a capacity of 1,046k bits. The FLEX10K50 and FLEX10K100 need 609k bits and 1,172k program bits downloaded, so we use 10 EPC1's in total. Seven EPC1's with a total capacity of $1,046\text{k} \times 7 = 7,322\text{k}$ bits are used for the group of FITTER chips, 6 FLEX10K100 with a $1,172\text{k} \times 6 = 7,032\text{k}$ bit memory requirement. Three EPC1's with a capacity of 3,138k bits are used for the controller chips, two FLEX10K100 and one FLEX10K50 devices with a total memory requirement of $2,953\text{k}$ bits.

LED The LED is the component that brightens the monitor LED's. The schematic is similar to that used in the L1 PreFred module [4]. The monitor LED's are defined in Table 4.

Table 4: The front panel LED's of the TF board.

Signal	Color	Position (ordered from top)	Comments
Power	red	top	SVT standard, AND of 3.3V and 5V.
VME Acknowledge	yellow	top	SVT standard.
SVT Init	red	middle	
SVT freeze	yellow	middle	
Clock	green	middle	
EPC1 Disable (Controller)	red	middle right	
EPC1 Disable (FITTER)	red	middle left	
HOLD (input)	red	w/ the input connector	SVT standard.
Data Strobe (input)	green	w/ the input connector	SVT standard.
HOLD (output)	red	w/ the output connector	SVT standard.
Data Strobe (output)	green	w/ the output connector	SVT standard.
CDF Error	red	bottom	SVT standard.
SVT Error	yellow	bottom	SVT standard.
RUN mode	green	bottom	SVT standard.

4 FEP (Front End Processor)

The top diagram of the FEP schematic is shown in Figure 5. The FEP consists of three components: the processor device (PROCESSOR), the input SPY buffer (ISPY), and the output buffer (TF FIFO). An ALTERA FLEX10K100ABC600-1 FPGA is used as the PROCESSOR.

4.1 PROCESSOR

The PROCESSOR controls reading data from the INPUT FIFO in the Front Panel and creating the TF word, which consists of five silicon hit positions and the XFT information. One TF word is produced for each possible combination of hits on a track. The PROCESSOR also controls writing the TF word into the TF_FIFO. The data flow in the PROCESSOR is shown in Figure 6. In the FEP stage, we save only the 8 LS bits of the SVX hit position as discussed in Section 2.2. The MS bits of the hit, discarded here, are reconstructible with the road ID.

All combinations of hits are processed by accessing all valid address in the memory in Figure 6. The simple diagram for addressing all possible combinations of hits is shown in Figure 7. In the example shown, we make a total of six (3×2) TF words.

To control the data flow, a state machine is used in the FEP. The simple diagram of the state machine is shown in Figure 8. The state transitions and their conditions are also shown in the figure. If SVT_INIT is detected, the state goes back to READY asynchronously. The number of hits in each layer is counted at the end of the DATA IN state. In the DATA OUT state, the proper memory address in each RAM is accessed to form all possible TF words. Due to hardware limitations, the TF keeps only the 8 LS bits of the SVX hit position, 1 bit of long cluster information[1], and the full XFT c and ϕ information. The number of hits per layer is also limited to 7 due to the hardware, which is same limitation as in the HB. We latch the input data in the Pre-DATA IN state. This state is necessary to control the readout of the INPUT FIFO road by road as shown in Figure 9. Latching the data also provides the necessary data set-up time for the following stage.

4.2 ISPY (Input Spy Buffer)

All of the SVT boards implement the SPY buffer system, which keeps a local copy of incoming and outgoing data. The SPY buffer is a memory with a circulating address pointer. After an error occurs anywhere in the SVT, the SPY address pointer is stopped by the SVT FREEZE signal on the backplane, and the error is analyzed after the SPY buffers are read out via VME. The ISPY (Input Spy Buffer) records the incoming data processed in the FEP. The ISPY is controlled by the PROCESSOR and is a single $128\text{k} \times 36$ memory, MOTOROLA MCM69F737. Since the typical input data is approximately 5 words per

[1] The long cluster bit for layer 2 is not stored in the RAM. Instead it is registered road by road due to a hardware limitation.

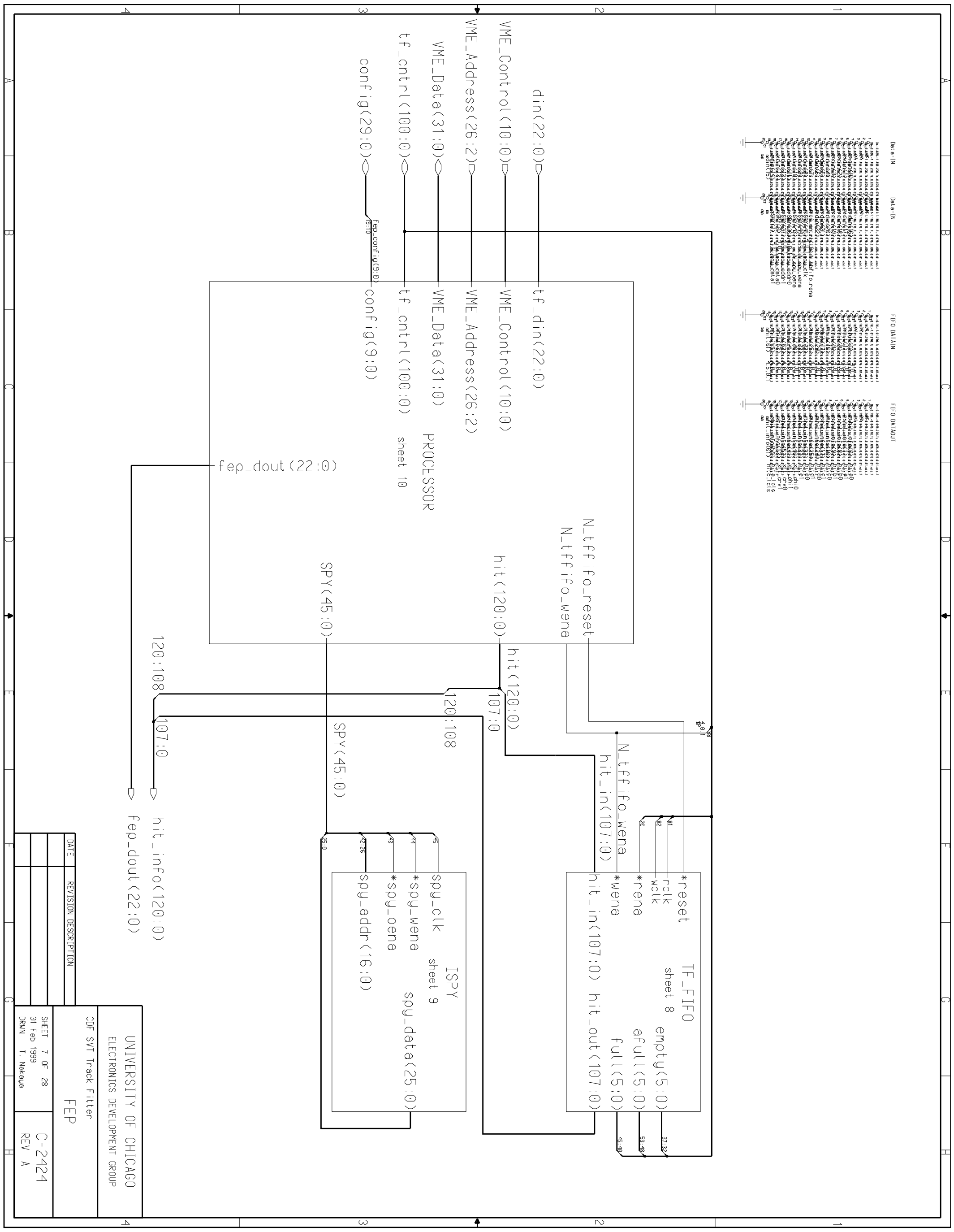


Figure 5: The top diagram of the FEP Schematic.

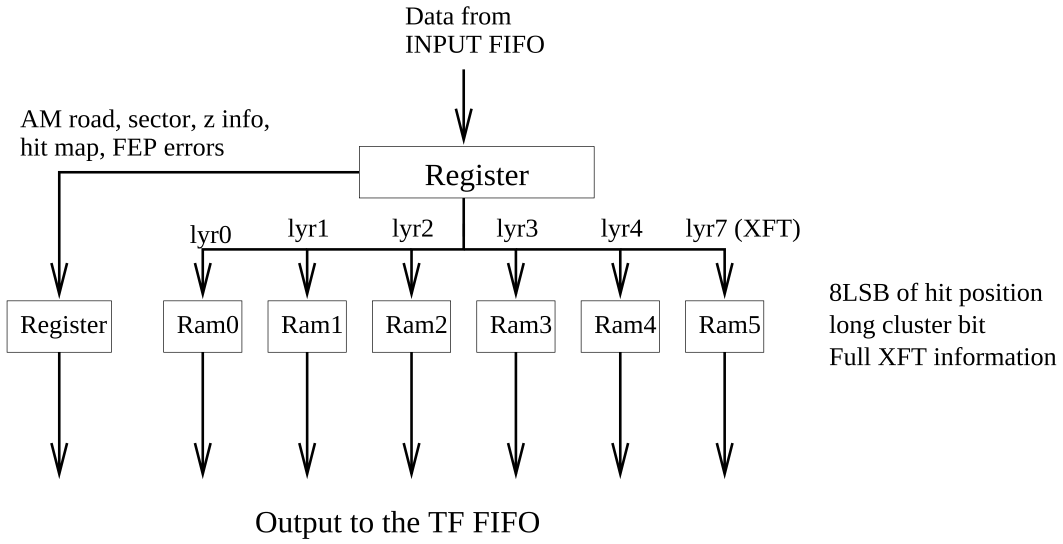


Figure 6: Diagram of the data flow in the FEP PROCESSOR. The incoming data are split based on the layer ID of the hit, and are stored in the corresponding RAM (Random Access Memory). At the end, all hit data are sent in parallel to the TF_FIFO for each possible combination. The AM road ID, the sector ID, the z information, the hit presence map and the error information in the FEP are registered and also sent to the TF_FIFO.

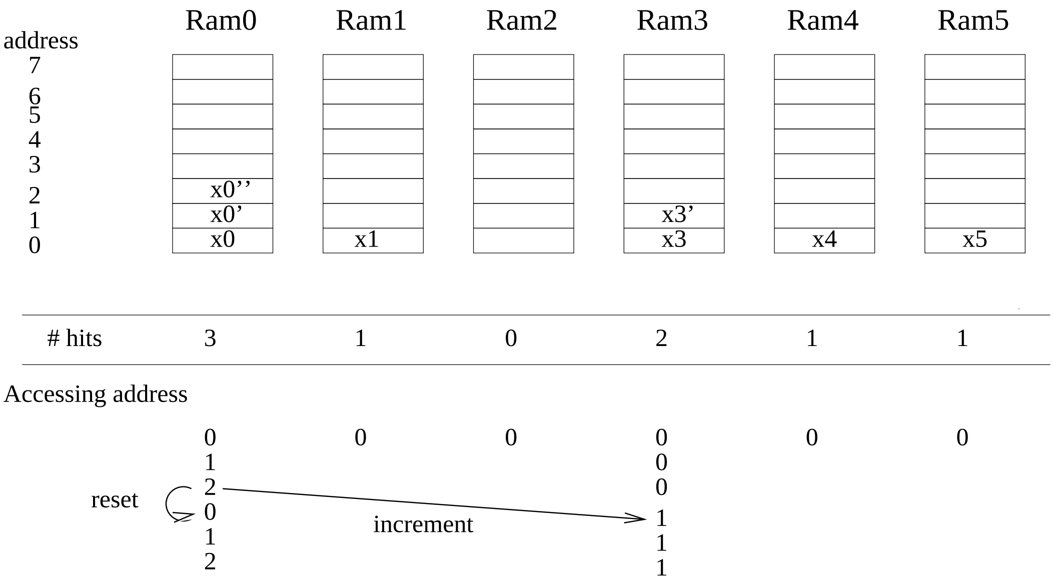
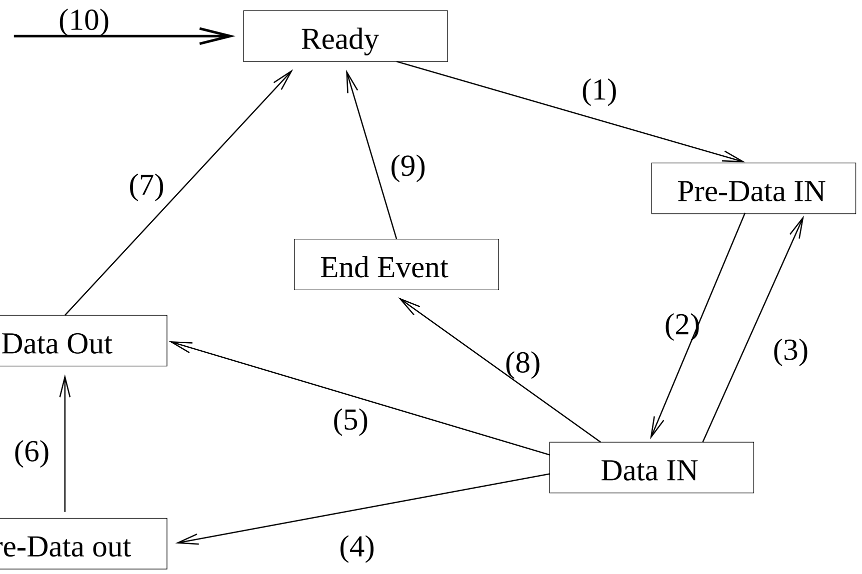


Figure 7: Diagram of the algorithm to address all possible combinations of hits for a track. The TF word contains data from six RAM's. In the Figure, we show the example of three hits in layer 0, two hits in layer 3, and one hit in the other layers except for layer 2 (no hit). In the figure, the address to Ram0 is increased every clock cycle with a counter. Once the counter reaches the number of hits in Ram0, the counter is cleared and one clock is sent to the counter for Ram3. When the counters for all Ram's reach the number of hits stored, all possible combinations of hits have been created. The TF words contain a garbage hit in layer 2, which has no hit. The garbage hit is ignored in the fitting stage by forcing the coefficient to be zero, i.e. $f_i(2) = 0$.



(1) INPUT FIFO is NOT EMPTY.
(2) INPUT FIFO is NOT EMPTY
(3) INPUT FIFO is EMPTY
(4) The EP (End Packet) is ON and TF_FIFO is FULL
(5) The EP (End Packet) is ON and TF_FIFO is NOT FULL.
(6) TF_FIFO is NOT FULL
(7) The end of permutation
(8) The EE (End Event) is ON
(9) The OPP sends the EE word.
(10) SVT_INIT is ON

Figure 8: The diagram of the state machine in the FEP to control the data flow. The EP (End Packet) signal defines the last word in the road. The EE (End Event) signal defines the last word in the event. The Pre-DATA IN state is necessary to control the readout of the INPUT FIFO road by road and to achieve long enough data set-up time in the FEP. Once the FEP receives the EE signal, the FEP waits for the downstream processor (OPP) to finish processing all track candidates.

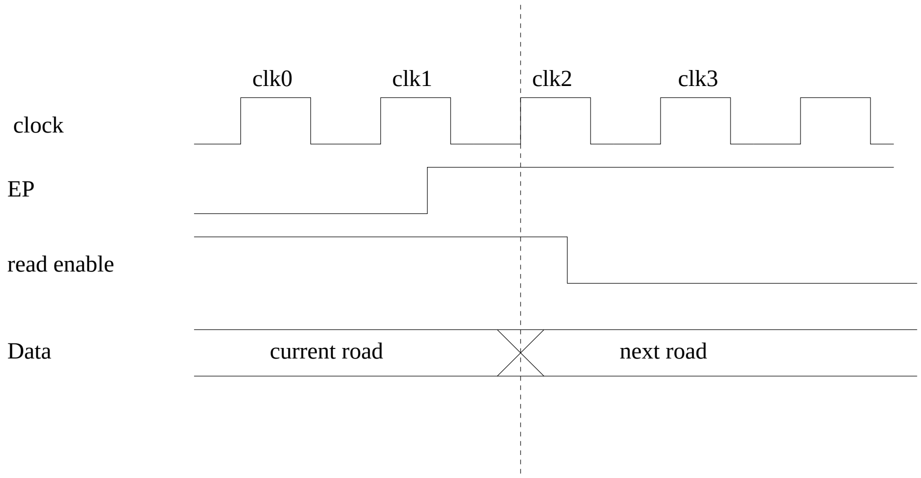


Figure 9: The method to control the INPUT FIFO readout. In the FEP, we read the data from the INPUT FIFO road by road. By the time the end of the road signal (EP) has been processed, the first word of the next road has already been read in. Therefore, that word has to be stored in a register in the FEP until the next road is ready to be processed.

event[2], the INPUT spy buffer can hold up to 25k events, which corresponds to almost a half second of data at the typical CDF L1 trigger rate. The details of the SPY buffer system are found in reference [3].

4.3 TF_FIFO (Buffer between the FEP and the FITTER)

The TF_FIFO is a buffer of the data between the FEP and the FITTER. With the TF_FIFO, the FITTER can run asynchronously from the FEP. The TF_FIFO is an array of CYPRESS 512×18 FIFOs, CY7C4215V. Since the data from the FEP to the FITTER are 99 bits wide, six FIFO's are required. The data into the TF_FIFO are listed in Table 5. Since the maximum number of roads per event is 63 according to the HB specification [3] and the average number of combinations per road is around 1.5, typically there are a maximum of 100 combinations per event. The 512 word FIFO thus includes a large safety factor.

5 FITTER

The top diagram of the FITTER schematic is shown in Figure 10. The FITTER consists of one control block (CNTRL) and six blocks for the arithmetic calculation (FITx). CNTRL manages the timing of the fitting process. In addition, CNTRL selects the proper fitting parameters for the best fit. We introduce each component in the following sections.

[2]The average number of roads per event is around 6 in all 12 wedges.

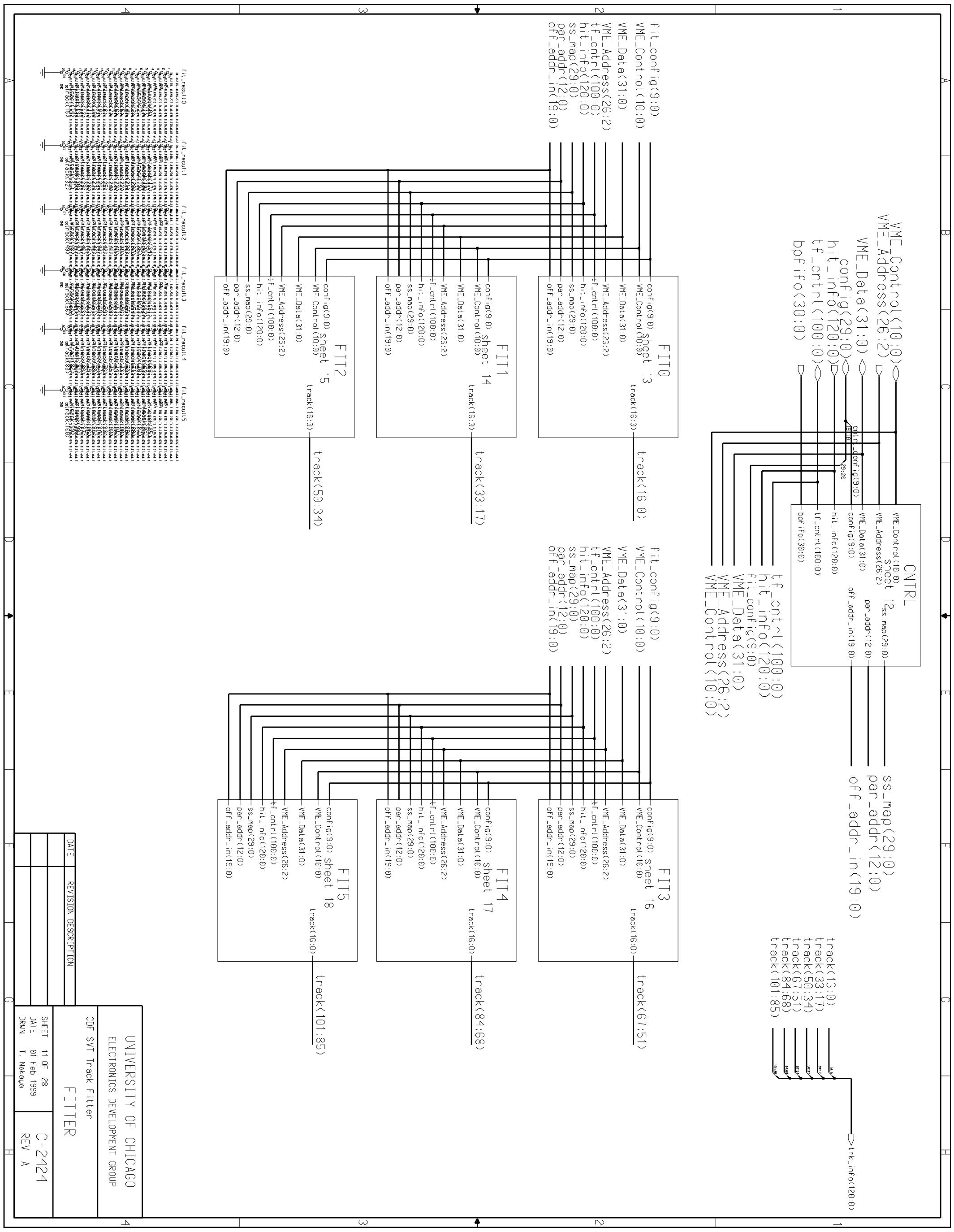


Figure 10: The top diagram of the FITTER Schematic.

Table 5: The data stored in the TF FIFO.

data	bits
The 8 LSBs of the hit position at layer 0	7- 0
The 8 LSBs of the hit position at layer 1	15- 8
The 8 LSBs of the hit position at layer 2	23-16
The 8 LSBs of the hit position at layer 3	31-24
The 8 LSBs of the hit position at layer 4	39-32
The XFT ϕ	51-40
The XFT c	58-52
The long cluster bit at layer 0	59
The long cluster bit at layer 1	60
The long cluster bit at layer 2	61
The long cluster bit at layer 3	62
The long cluster bit at layer 4	63
The hit presence map of the layers	69-64
The z barrel ID for the innermost hit	72-70
The z barrel ID for the outermost hit	75-73
The AM road ID	90-76
The sector ID	94-91
The error information in the FEP	99-95

5.1 CNTRL

The CNTRL block consists of one FPGA and two memories. The FPGA, called the CNTRL chip, is an ALTERA FLEX 10K50VBC356-3. It manages the schedule for the fit calculation and the memory access. One memory, SS_MAP, is used to get the edge position of the SS in the AM road. The other memory, MAKE_ADDR, is used to select the correct fitting parameters for a set of hit layers, long clusters, and barrels. The output from MAKE_ADDR is the addresses to the Intercept memory and the Coefficient memory described in Section 5.2.

In the CNTRL chip, a simple state machine manages the fit starting and ending times with three states: READY, RUN and DONE. The state is READY whenever SVT INIT arrives. The state changes from the READY to RUN when TF_FIFO goes NOT EMPTY. In the RUN state, the READ ENABLE signal to the TF_FIFO is sent for one clock cycle and then the CNTRL chip starts counting the number of clocks. When the number reaches the programmed value (called the target number), the state moves from RUN to DONE, and the "FIT_DONE" signal is generated. This delay is the time needed for the fit calculation. The target number is recorded inside the chip and is programmable through VME. With a 30 MHz clock, the target number should be 8 or larger since it takes 250 nsec to get a stable result from the calculation. The range of the target number is from 1 to 31, but must not be 0. In the RUN state, if the OPP processor is busy sending data (OPP busy), or if the HOLD signal is detected from downstream (OUTPUT cable), the state transition is inhibited even if the count reaches the target number. The state transition will occur as soon as the OPP busy or the Hold signal is cleared. The operation of the CNTRL chip is synchronized with that of the OPP.

In addition to the function of the state machine, the CNTRL chip sets the proper addresses to the SS_MAP and MAKE_ADDR memories. The SS_MAP memory contains the edge position of the SS in the AM road. The address to the memory is the AM road ID whose range is from 0 to 32k (15 bits). In the TF, we need only the lower 4 bits of the SS position since we use only 8 bits of hit position in the arithmetic calculation[3]. The output data have 4 bits of SS position per layer; they are thus $4 \times 6 = 24$ bits wide in total. We use a MOTOROLA MCM69F536C 32k $\times$ 36 synchronous memory. The function of the MAKE_ADDR memory is to select the correct fitting parameters, f_i , out of many combinations with many fitting conditions. The fitting parameters depend on the presence of a hit for each layer (hit map), the presence of the long cluster bit for each hit (long cluster map), and the z barrel ID of the innermost hit. For example, we need five different sets of fitting parameters for the five combinations in which four SVX layers are selected out of the five physical layers. In addition, even after selecting the four SVX layers, the selection of the fitting parameters also depends on whether a hit is a long cluster or not. We prepare fitting parameters to allow one hit with a long cluster per road. The fitting parameters also depend on the z ID of the hit. The address for this memory consists of the 6 bits of the hit map, 5 bits of the long cluster map and 3 bits of Z ID for the innermost hit. The output is the address to the Coefficient memory and the sub-address to the Intercept memory described in Section 5.2. The simple functional diagram of the MAKE_ADDR memory is shown in Figure 11.

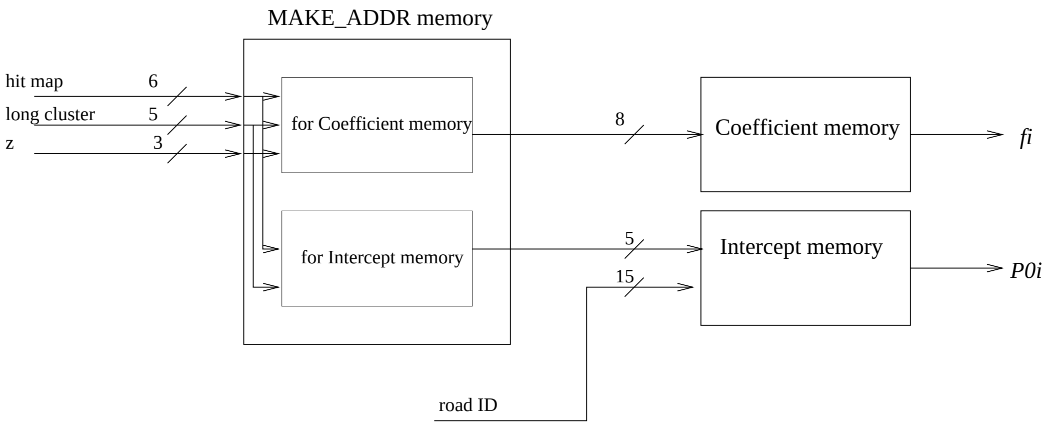


Figure 11: The function of the MAKE_ADDR memory which creates addresses to the Coefficient memory and the Intercept memory.

[3]The SS position is the upper 10 bits out of the 14-bit hit information

5.2 FIT

In the FIT block, we perform the track fit of Equations 1 and 2. The track parameters at the edge of the SS position in the AM road ($p0_i$ in Equation 3) are provided by memory lookup in an INTEL 1M $\times$ 16 FlashFile memory 28F160S3 (Intercept memory). The arithmetic calculation in Equation 4 is performed with the ALTERA FLEX10K100ABC356-1 chip (FIT). The coefficients of the multiplication in Equation 4, f_i, are provided by the embedded memory inside the FIT chip (Coefficient memory). Since we calculate three track parameters and three constraints at the same time, we have 6 sets of the FIT chip and the Intercept memory. The FIT0, FIT1, FIT2, FIT3, FIT4 and FIT5 symbols in Figure 10 correspond to the calculations of ϕ, d, c, χ_1, χ_2 and χ_3, respectively.

Each FIT chip performs the arithmetic calculation shown in Figure 12. In Figure 12,

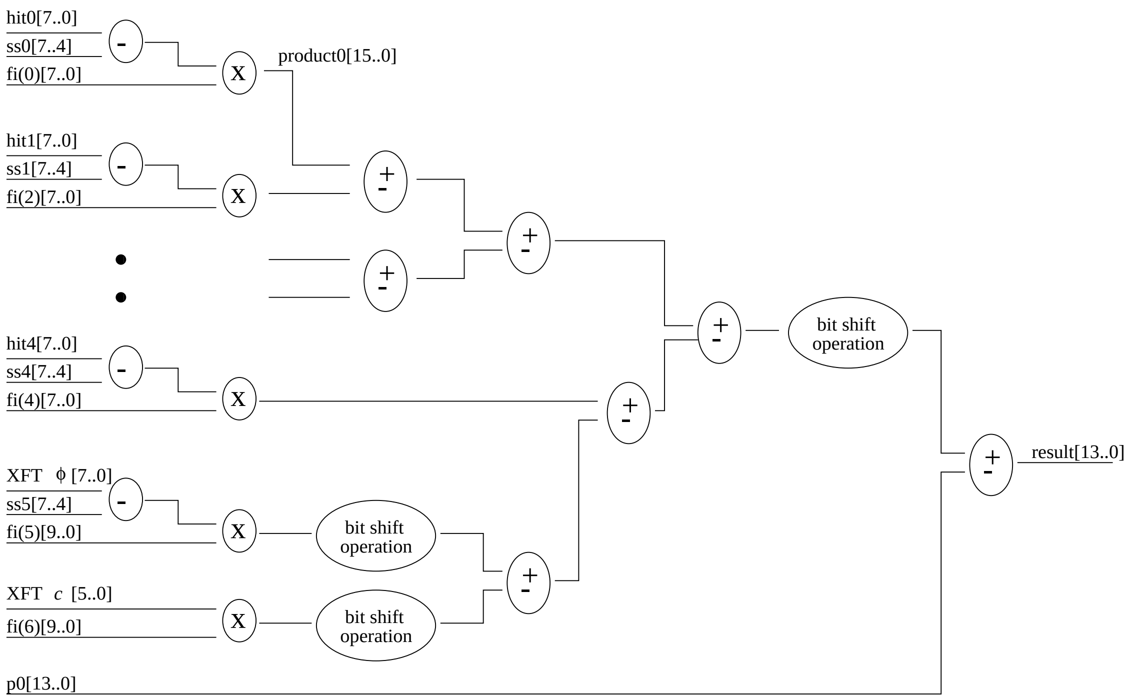


Figure 12: The diagram of the calculation in the FIT chip. At each bit shift operation, the overflow is monitored.

we first subtract the SS edge from the hit position. Then we calculate the product of the coefficient times the hit position in the SS. At the next stage, we perform a bit shift operation on the XFT products if it is necessary to get better resolution. Then, we sum up all the products except for the $p0_i$ value in Equation 2. A bit shift operation is executed on the sum, and finally the $p0_i$ value is added. At each stage, we monitor the overflow bit and send it to the OPP chip, which monitors error conditions. The bit counts in the two shift operations depend on the fitting parameters, but do not vary event by event. For example, in the calculation of d, we shift the XFT ϕ product by 3 bits, the XFT c product by -3 bits, and the final result by 2 bits. The output of the result is 14 bits wide with the sign as the MSB. In addition, we generate three bits of overflow information as output. In total, one (six) FIT chip sends 17 (102) bits of output data.

The Intercept memory stores the pre-calculated values of Equation 3. The address to the memory includes the AM road ID (15 bits). In addition, the address also includes the output from the MAKE_ADDR memory to select the best fit parameters. The AM road ID itself includes information on the z ID of hits. Therefore, the sub-address from the MAKE_ADDR memory does not depend on the z ID, but depends on the hit map (6 bits) and the long cluster map (5 bits). There are 5 patterns in the hit map to select 4 SVX layers: (0,1,1,1,1), (1,0,1,1,1), (1,1,0,1,1), (1,1,1,0,1) and (1,1,1,1,0). In addition, there are another 5 patterns in the long cluster map to select the best fit parameters: (0,0,0,0), (1,0,0,0), (0,1,0,0), (0,0,1,0) and (0,0,0,1). In total, we select the best fit parameters out of $5 \times 5 = 25$ combinations, which is expressed with 5 bits. In total then, the address of the Intercept memory is $15 + 5 = 20$ bits wide. The data from the Intercept memory are the pre-calculated values of Equation 3, which are 14 bits wide with the sign as the MSB.

The coefficient memory stores the contents of the $\vec{f_i}$ in Equation 4. The fitting parameters are chosen based on the hit map of the layers (6 bits), the map of the long clusters (5 bits) and the z ID of the innermost hit (3 bits). As mentioned for the Intercept memory, we have 25 patterns based on the hit map and the long cluster map. In addition, there are another 6 patterns due to the z ID. In total, we have 150 $\vec{f_i}$ in this memory. The contents of the $\vec{f_i}$ are 9 bits wide for each SVX layer and 11 bits wide for the XFT ϕ and c, all of which include the sign bit. In total, the width of the data is $9 \times 5 + 11 \times 2 = 67$ bits wide. Since we have to access the memory through the 32-bit VME data bus, the Coefficient memory is divided into three parts.

6 OPP (OutPut Processor)

The top diagram of the OPP schematic is shown in Figure 13. The OPP consists of three components: the processor device (PROCESSOR), the output SPY buffer (OSPY), and the FIFO to store the part of the outgoing data used to find the beam position.

6.1 PROCESSOR

The main function of the OPP PROCESSOR is to collect the results from six FIT chips, to apply a fit quality cut on the value of each of the three constraints, to calculate the χ^2, and to handle error conditions. An ALTERA FLEX10K100ABC600-1 is used for the PROCESSOR.

The OPP has a simple state machine. When the "FIT_DONE" signal (see Section 5.1) is detected, the OPP latches the results from the FIT chips, 8 LSB of hit position at each layer, the road ID, the sector ID, the z information and the error information. Then, the OPP constructs the 7 SVT words defined in Table 2. The OPP calculates the parity of the

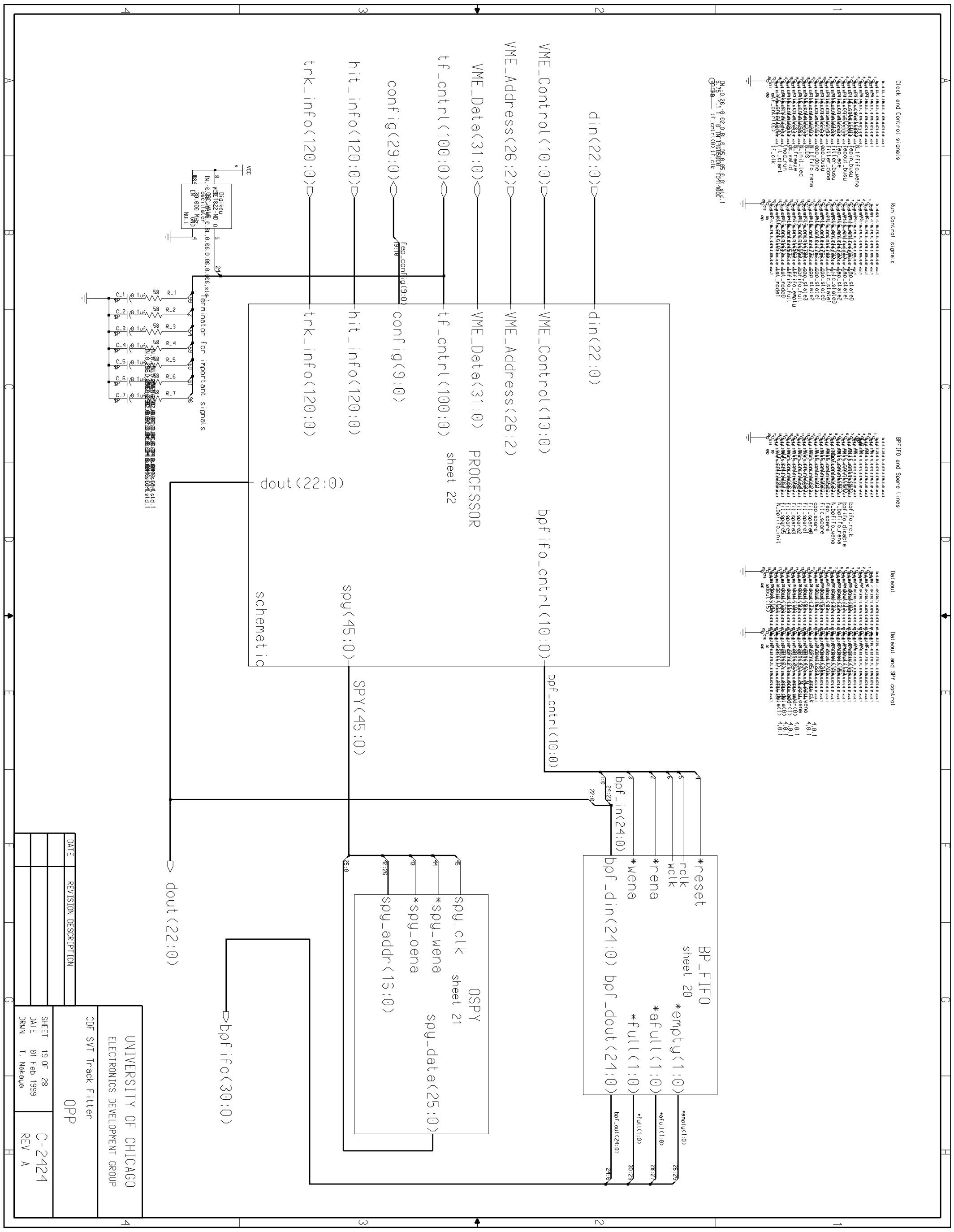


Figure 13: The top diagram of the OPP Schematic.

words, which is the bitwise XOR of all out-going data words in the event excluding the End of Event word. If the fit quality cut is passed, the OPP starts sending the SVT words clock by clock.

The fit quality cut is the simple comparison of each χ_i value with the cut value. We use only bits 7 to 2 in the χ_i for the comparison, where the LSB of the χ_i corresponds to 0.5. If each χ_i is smaller than its cut value, the fit quality cut is passed. As an option, we can disable the fit quality cut through VME (see Table 6).

The OPP simultaneously performs the χ^2 calculation: $\chi^2 = \chi_1^2 + \chi_2^2 + \chi_3^2$. To calculate the square of χ_i, we simply do a memory lookup using the embedded memory in the OPP chip. We only use the lowest 6 bits in the χ_i to calculate the square. The range of the input to the square memory is 0 to 31.5 with a LSB of 0.5, and the range of the output from the memory is 0 to 992 with a LSB of 1. The three χ_i^2 values are added, resulting in 11 bits of χ^2 ranging from 0 to 1023 with one overflow bit.

The OPP also controls error handling. The OPP summarizes the error status of the fit before sending the output data. If an unmasked error is detected, the OPP sends the data even if the event does not pass the track quality cut. In addition, the OPP pulls the CDF ERROR and the SVT ERROR depending on the error type. The error handling in the TF is more fully discussed in Section 8.

6.2 OSPY (Output Spy Buffer)

The OSPY is very similar to the ISPY system. Since he OPP sends the data off of the TF board, the OPP has a SPY buffer (OSPY=Output Spy Buffer) as mentioned in Section 4.2. We use the same MOTOROLA MCM69F737 memory as in the ISPY.

The address pointer to the OSPY is circulating, and is frozen when the SVT FREEZE signal is detected. The typical output data is approximately 2 words per event per sector. The OSPY can hold up to 60k events which corresponds to approximately one second of data.

6.3 BP_FIFO (for beam position finding)

The BP_FIFO is a set of FIFO's to store information need for finding the beam position. We use two CYPRESS CY7C4285V 64k $\times$ 18 FIFO's. The information stored is the first two SVT words in Table 2, which contain the z, ϕ, curvature and impact parameter of each track passing the fit quality cuts. The 20th bit of the first output word is set to ONE to identify the first word in a pair in the BP_FIFO. The 20th bit of the second output word is ZERO. Through VME, we can read the data in the BP_FIFO any time. The FIFO status is attached to the data in a VME read. Bits 25, 26, 27, 28, 29 and 30 are NOT empty in one FIFO, NOT empty in the other, NOT almost full in one and the other, and NOT full in one and the other, respectively. We can also clear these FIFO's anytime through VME.

Since the BP_FIFO is 64k deep, it can keep up to 32k tracks per sector.

7 VME Interface and Accessible VME Address

The VME Interface is very similar to those in the CDF L1 PreFred board and the CrateSum board. The description of the program in the VME interface chip to carry out the 32-bit data transfers can be found in the L1 documents [4, 5].

In the TF, four SVT special signals are connected to the VME P2 backplane: SVT_INIT, SVT_ERROR, SVT_FREEZE, and SVT_SPARE on pins A1, A2, A3 and A5, respectively. Among the CDF standard control signals on the P2 backplane, only the CDF_ERROR signal is used in the TF.

The VME commands in the TF board are listed in Tables 6, 7, and 8. The memory accessible through VME is also listed in Table 9. The VME address lines from the VME interface chip and the VME data lines go to all 9 FPGA chips in the TF.

8 Error Handling and Track Fitter Status Word

Possible TF errors and their location in the ERROR register are shown in Table 10. The state of the ERROR register is used to generate SVT_ERROR, CDF_ERROR, the TF status word in the output data stream, and the error flags in the end of event (EOE) word. For each of these, errors in the ERROR register may be masked off. The VME addresses of the MASK words are given in Table 8. The MASK words for SVT_ERROR, CDF_ERROR, and the TF status word have the same structure as the ERROR register. The MASK word for the EOE word has the same structure as the SVT standard 10-bit EOE error flag defined in Table 11. The TF pulls CDF_ERROR only when a FIFO overflow occurs. In addition, the FIFO overflow is persistent in the SVT EOE word. Therefore, once it occurs, the TF continues to generate the error until a reset signal is received.

SVT protocol requires that when SVT_INIT is received, CDF_ERROR, SVT_ERROR and the ERROR register are cleared. In the TF, there are two identical ERROR registers: one (ERROR Register 1) is cleared by SVT_INIT, while the other (ERROR Register 2) is not. ERROR Register 2 is only cleared by a VME write. Thus ERROR Register 1 is sensitive to the most recent error which caused either CDF_ERROR or SVT_ERROR, while ERROR Register 2 contains the integration of error conditions. This is useful if SVT_INIT is sent immediately after a CDF_ERROR in order to minimize data taking dead time. In that case, ERROR Register 2 holds the error condition for later analysis.

The error summary for each fit is contained in the TF status word, which is defined in Table 12. In addition to the error information, the TF status word also contains the HIT status word that is sent from the Level-2 SVT interface board to the Level-2 processors. Encoded in these 4 bits are the silicon layers with hits on the track and the layers whose hits are wide clusters. The mapping of this data is not yet defined and can be loaded into the board via VME transfer.

Table 6: VME Commands and addresses on the TF board -1. The data bits not defined here should be masked by the user.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x0000000	r/w	any time	bit0 : run_mode
0x0000004	r/w	NOT run mode	bit1-0: test mode type, bit5-2: TF ID, bit15-6: #events tried in test_mode, bit16 : run test mode, bit17 : select VME clock, bit18 : select 1/2 on-board clock, bit19 : on-board clock disable, bit20 : generate FREEZE, bit21 : generate INIT.
0x0000008	r/w	NOT run_mode	bit4-0: Max. trials for permutation, bit7-5: Min. hits requirement. bit8: INPUT_FIFO read disable.
0x000000C	r/w	NOT run_mode	bit4-0: χ_1 cut value ($\times 2$), bit 5: do χ_1 cut, bit10-6: χ_2 cut value ($\times 2$), bit 11: do χ_2 cut, bit16-12: χ_3 cut value ($\times 2$), bit 17: do χ_3 cut. bit18 : BP_FIFO write is debug mode (all SVT words are written).
0x0000010	r/w	NOT run_mode	bit4-0: Clock counts to the FIT_DONE. bit5: TF_FIFO read disable. bit6: BP_FIFO write disable.
0x0000014	r/w	NOT run_mode	bit4-0: bit shift distance for the ϕ, bit9-5: bit shift distance to add the XFT ϕ product, bit14-10: bit shift distance to add the XFT c product note: each MSB is the shift direction
0x0000018	r/w	NOT run_mode	same definition as 0x0000014 for the d.
0x000001C	r/w	NOT run_mode	same definition as 0x0000014 for the c.
0x0000020	r/w	NOT run_mode	same definition as 0x0000014 for the χ_1.
0x0000024	r/w	NOT run_mode	same definition as 0x0000014 for the χ_2.
0x0000028	r/w	NOT run_mode	same definition as 0x0000014 for the χ_3.
0x000002C	r/w	w/ freeze	ISPY counter (write: reset) bit16-0: pointer, bit17: overflow, bit18: SPY status (Freeze=0)
0x0000030	r/w	w/ freeze	OSPY counter (write: reset) bit16-0: pointer, bit17: overflow, bit18: SPY status (Freeze=0)
0x0000034	r	NOT run_mode	bit4-0: FEP program version number
0x0000038	r	NOT run_mode	bit4-0: OPP program version number
0x000003C	r	NOT run_mode	bit4-0: FITTER/CONTROL program version number
0x0000040	r	NOT run_mode	bit4-0: FITTER/FIT0 program version number
0x0000044	r	NOT run_mode	bit4-0: FITTER/FIT1 program version number
0x0000048	r	NOT run_mode	bit4-0: FITTER/FIT2 program version number
0x000004C	r	NOT run_mode	bit4-0: FITTER/FIT3 program version number
0x0000050	r	NOT run_mode	bit4-0: FITTER/FIT4 program version number
0x0000054	r	NOT run_mode	bit4-0: FITTER/FIT5 program version number

Table 7: VME Commands and addresses on the TF board -2.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x0000058	r	NOT run_mode	INPUT FIFO read bit22-0 : SVT input data, bit23 : input HOLD.
0x000005C	r	NOT run_mode	TF FIFO (bits 90-59) at FITTER/CONTROL
0x0000060	r	NOT run_mode	TF FIFO (bits 99-91) at FITTER/CONTROL
0x0000064	r	NOT run_mode	bit2-0: FITTER/FIT0 ID (must be 0)
0x0000068	r	NOT run_mode	bit2-0: FITTER/FIT1 ID (must be 1)
0x000006C	r	NOT run_mode	bit2-0: FITTER/FIT2 ID (must be 2)
0x0000070	r	NOT run_mode	bit2-0: FITTER/FIT3 ID (must be 3)
0x0000074	r	NOT run_mode	bit2-0: FITTER/FIT4 ID (must be 4)
0x0000078	r	NOT run_mode	bit2-0: FITTER/FIT5 ID (must be 5)
0x000007C	r	NOT run_mode	TF_FIFO (bits 31-1) read by FIT0
0x0000080	r	NOT run_mode	TF_FIFO (bits 31-1) read by FIT1
0x0000084	r	NOT run_mode	TF_FIFO (bits 31-1) read by FIT2
0x0000088	r	NOT run_mode	TF_FIFO (bits 31-1) read by FIT3
0x000008C	r	NOT run_mode	TF_FIFO (bits 31-1) read by FIT4
0x0000090	r	NOT run_mode	TF_FIFO (bits 31-1) read by FIT5
0x0000094	r	NOT run_mode	TF_FIFO (bits 58-32) read by FIT0
0x0000098	r	NOT run_mode	TF_FIFO (bits 58-32) read by FIT1
0x000009C	r	NOT run_mode	TF_FIFO (bits 58-32) read by FIT2
0x00000A0	r	NOT run_mode	TF_FIFO (bits 58-32) read by FIT3
0x00000A4	r	NOT run_mode	TF_FIFO (bits 58-32) read by FIT4
0x00000A8	r	NOT run_mode	TF_FIFO (bits 58-32) read by FIT5
0x00000AC	r	NOT run_mode	FIFO status bit1-0 : NOT EMPTY of INPUT FIFO, bit7-2 : NOT EMPTY of TF_FIFO, bit9-8 : NOT Half FULL of INPUT FIFO, bit15-10 : NOT Half FULL of TF_FIFO, bit17-16 : NOT FULL of INPUT FIFO, bit23-18 : NOT FULL of TF_FIFO,

Table 8: VME Commands and addresses on the TF board -3. The fitting result read by the OPP consists of 14 bits of data plus 3 bits of overflow error information.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x00000B0	r/w	NOT run_mode OR SVT_Freeze	Error Status Register-1 (reset by the SVT INIT) read bit10-0 : error status write bit0 : clear the register write bit1 : clear the SVT ERROR write bit2 : clear the CDF ERROR
0x00000B4	r/w	NOT run_mode OR SVT_Freeze	Error Status Register-2 (NOT reset by the SVT INIT) read bit10-0 : error status read bit31 : CDF_ERR presents, bit30 : SVT_ERR presents write bit0 : clear the register write bit1 : clear the SVT ERROR write bit2 : clear the CDF ERROR
0x00000B8	r/w	NOT run_mode	bit10-0: TF Error MASK
0x00000BC	r/w	NOT run_mode	bit10-0: SVT Error MASK
0x00000C0	r/w	NOT run_mode	bit10-0: CDF Error MASK
0x00000C4	r/w	NOT run_mode	bit9-0: EOE word Error MASK
0x00000C8	r	NOT run_mode	bit16-0: ϕ result at OPP
0x00000CC	r	NOT run_mode	bit16-0: d result at OPP
0x00000D0	r	NOT run_mode	bit16-0: c result at OPP
0x00000D4	r	NOT run_mode	bit16-0: χ_1 result at OPP
0x00000D8	r	NOT run_mode	bit16-0: χ_2 result at OPP
0x00000DC	r	NOT run_mode	bit16-0: χ_3 result at OPP
0x00000E0	r/w	NOT run_mode	generate a single clock based on the VME data strobe.

Table 9: VME Addresses to the memories.

Address(26:0)	Operation	Access condition	Command (VME Data)
0x0001xxx	r/w	NOT run_mode	FIT0 Coefficient memory (bit 31-0)
0x0002xxx	r/w	NOT run_mode	FIT1 Coefficient memory (bit 31-0)
0x0003xxx	r/w	NOT run_mode	FIT2 Coefficient memory (bit 31-0)
0x0004xxx	r/w	NOT run_mode	FIT3 Coefficient memory (bit 31-0)
0x0005xxx	r/w	NOT run_mode	FIT4 Coefficient memory (bit 31-0)
0x0006xxx	r/w	NOT run_mode	FIT5 Coefficient memory (bit 31-0)
0x0007xxx	r/w	NOT run_mode	FIT0 Coefficient memory (bit 63-32)
0x0008xxx	r/w	NOT run_mode	FIT1 Coefficient memory (bit 63-32)
0x0009xxx	r/w	NOT run_mode	FIT2 Coefficient memory (bit 63-32)
0x000Axxx	r/w	NOT run_mode	FIT3 Coefficient memory (bit 63-32)
0x000Bxxx	r/w	NOT run_mode	FIT4 Coefficient memory (bit 63-32)
0x000Cxxx	r/w	NOT run_mode	FIT5 Coefficient memory (bit 63-32)
0x000Dxxx	r/w	NOT run_mode	FIT0 Coefficient memory (bit 67-64)
0x000Exxx	r/w	NOT run_mode	FIT1 Coefficient memory (bit 67-64)
0x000Fxxx	r/w	NOT run_mode	FIT2 Coefficient memory (bit 67-64)
0x0010xxx	r/w	NOT run_mode	FIT3 Coefficient memory (bit 67-64)
0x0011xxx	r/w	NOT run_mode	FIT4 Coefficient memory (bit 67-64)
0x0012xxx	r/w	NOT run_mode	FIT5 Coefficient memory (bit 67-64)
0x0013xxx	r/w	NOT run_mode	χ^2 Memory bit 9-0: Square of (address i/2).
0x01xxxxx	r	any time	ID PROM (see CDF note xxxx).
0x04xxxxx	r/w	freeze	ISPY memory bit 22-0: SVT data, bit 23: HOLD
0x05xxxxx	r/w	freeze	OSPY memory bit 22-0: SVT data, bit 23: HOLD
0x060xxxx	r/w	NOT run_mode	SS_MAP memory bit 3-0: 4 LSB of SS position at layer 0. bit 7-4: 4 LSB of SS position at layer 1, and so on
0x068xxxx	r/w	NOT run_mode	MAKE_ADDR memory bit 4-0: Sub-address to the Intercept memory. bit 12-5: Address to the Coefficient memory.
0x0700000	r/w	any time	read BP_FIFO, or write: Reset the FIFO bit 22-0: SVT data. bit 24-23: spare bit 30-25: FIFO flags. (FF1, FF2, AF1, AF2, EF1, EF2) EF1 is the empty flag of FIFO-1, and AF and FF is the almost Full and Full flags. Flags are active low.
0x40xxxxx	r/w	NOT run_mode	Intercept Memory for FIT0 bit 12-0: Intercept, bit 13: sign
0x48xxxxx	r/w	NOT run_mode	Intercept Memory for FIT1
0x50xxxxx	r/w	NOT run_mode	Intercept Memory for FIT2
0x58xxxxx	r/w	NOT run_mode	Intercept Memory for FIT3
0x60xxxxx	r/w	NOT run_mode	Intercept Memory for FIT4
0x68xxxxx	r/w	NOT run_mode	Intercept Memory for FIT5

Table 10: The definition of the ERROR Register in the TF. The TF has two identical ERROR Registers: one (Register-1) is cleared by SVT_INIT and the other (Register-2) is not.

ERROR register	Error	Comment
bit 0	parity error	parity mismatch in the input data
bit 1	hit overflow	#hits/layer is overflowed (>7)
bit 2	less hit	#hits/road is too small ($<$ Min. hits requirement.)
bit 3	out of order	hits arrive out of order
bit 4	comb. overflow	# of hit combinations is too large ($>$ Max. trials for permutation).
bit 5	layer overflow	too many layers with multiple hits (>4)
bit 6	INPUT FIFO full	INPUT FIFO is full
bit 7	TF_FIFO full	TF FIFO is full
bit 8	XFT ϕ overflow	The XFT ϕ product overflow
bit 9	XFT c overflow	The XFT c product overflow
bit 10	FIT overflow	The FIT result overflow

Table 11: The definition of the End of Event ERROR word in the SVT.

ERROR word	Error	validity	ERROR Register bit	Comment
bit 0	parity error	Yes	0	
bit 1	Lost Sync	No		
bit 2	FIFO Overflow	Yes	6, 7	pull CDF error
bit 3	Invalid Data	Yes	2, 3	
bit 4	Internal Overflow	Yes	1, 4, 5, 8, 9, 10	
bit 5	Truncated Output	No		
bit 6	G-link Lost Lock	No		
bit 9-7	spare			

Table 12: The definition of the TF status word

TF status	Comment
bit 3-0	Hit status word.
bit 4	unused
bit 5	hit overflow.
bit 6	layer overflow.
bit 7	comb. overflow.
bit 8	Invalid data (“less hit” OR “out of order”)
bit 9	overflow in the fit (XFT ϕ OR c OR FIT overflow)
bit 10	FIFO overflow
bit 11	OR of all error bits after the MASK.

9 Test Mode

The TF has four types of test modes as shown in Table 13. Test modes are not active unless the run mode bit is OFF. When the TF is set to Test Mode 1, the TF generates an extra word to separate the original output data from the attached input data. The word for the separation is data$(22:0)$ = 0x3FFFFF, in which all SVT word bits are ON except for the EE bit. This word is included even if there is no input data because the INPUT FIFO is empty. For Test Modes 2 and 3, the “run test_mode” bit must be set ON (bit 16 in VME word 0x0000004 as shown in Table 6). At the next clock cycle after setting the “run test_mode” bit ON, the test mode starts running. In order to run the test mode with a finite number of events, set the number of trials for the test in the same register. The test stops when the number of events reaches the number set in the register. Note that the number of trials must be set before the “run test_mode” bit is turned ON. If the number of trials is set to zero, test mode will continue running until the “run test_mode” bit is turned OFF through VME. For the test_mode clock, either the on-board clock or a clock based on the VME data strobe may be selected. To select the VME clock, disable the on-board clock and select the VME clock using bits 17 and 18 in VME address 0x0000004. Once the register is set properly, when VME address 0x00000E0 is accessed (read or write), the clock is generated with the same timing as the VME data strobe.

Table 13: The definition of the test_modes in the TF.

Test Mode bit(1:0)	Function
0	same as run_mode except for the possibility of VME access.
1	include the input data in the TF output.
2	The ISPY data are used as the TF input.
3	The OSPY data are used as the TF output.

10 Performance and Remarks

The processing time of the TF is approximately expressed as

$$\mathrm{T_{TF}} \;=\; 1.0 + 0.3 \times \#\text{combinations} \times (\#\text{roads} - 1)\ [\mu\text{sec}] : \tag{5}$$

For a typical event with 5 roads and with 1.5 combinations per road, the processing time of the TF is expected to be $1.0 + 0.3 \times 1.5 \times (5 - 1) = 2.8\mu$sec. For an event with no road, the TF finishes processing in 5 clock cycles, or 165 nsec. Changing the fitting parameters in the TF requires reloading the Flash File memory (Intercept Memory). Since the memory is not fast and is big (16Mbits $\times$ 6), it is not practical to change the fitting parameters run by run.

References

[1] S. Belforte et al, "SVT Silicon Vertex Tracker TECHNICAL DESIGN REPORT", CDF NOTE. 3108 (1996).

[2] S. Belforte et al, "Specification of the XFT, SVT, and Level 2 Interfaces", CDF NOTE. 4578 (1996).

[3] S. Belforte et al, "Hit Buffer Specifications and Design", SVT internal note. 51 (1996).

[4] A. Amadon et al, "Specifications and Design of the Level 1 Calorimeter Trigger Pre-FRED Modules for the RUN II Upgrade.", CDF NOTE. 4340 (1997).

[5] Nancy J. Lai and D. Toback, "CrateSum Board Design Document", CDF NOTE 4812 (1998).

A Schematics, Board Layout and Parts list

The schematics of the TF board are composed of 28 sheets. The postscript files of the schematics are available at the URL "http://fozzie.uchicago.edu/ nakaya/schematics.html" or the directory "/designs/CDF_SVT/Track_Fitter/fig/schematics/" on the UNIX machine in the E-shop at the University of Chicago. The content of each sheet is summarized in Table 14.

Table 14: The content of each sheet in the TF schematics.

sheet 1	top view
sheet 2	Front Panel (FP) View
sheet 3	FP/LED View
sheet 4	FP/CONFIG View
sheet 5	FP/DATAIN View
sheet 6	FP/DATAOUT View
sheet 7	Front End Processor (FEP) View
sheet 8	FEP/TF_FIFO View
sheet 9	FEP/ISPY View
sheet 10	FEP/PROCESSOR View
sheet 11	FITTER top view
sheet 12	FITTER/CONTROL View
sheet 13	FITTER/FIT0 View
sheet 14	FITTER/FIT1 View
sheet 15	FITTER/FIT2 View
sheet 16	FITTER/FIT3 View
sheet 17	FITTER/FIT4 View
sheet 18	FITTER/FIT5 View
sheet 19	OutPut Processor (OPP) top View
sheet 20	OPP/BP_FIFO View
sheet 21	OPP/OSPY View
sheet 22	OPP/PROCESSOR View
sheet 23	TF_VME_Interface View
sheet 24	VME Interface View
sheet 25	VME P1 Bus View
sheet 26	VME P0 Bus View
sheet 27	VME P2 Bus View
sheet 28	Power

The board layout is shown in Figure 14.

Finally, the parts list is shown in Figure 15.

B Power

On the TF board, there are two power lines: 5V and 3.3V. We use 3.3V for all FLEX 10K chips, and 5V for the MAX chip. Most of the drivers, multiplexers, receivers, oscillator,

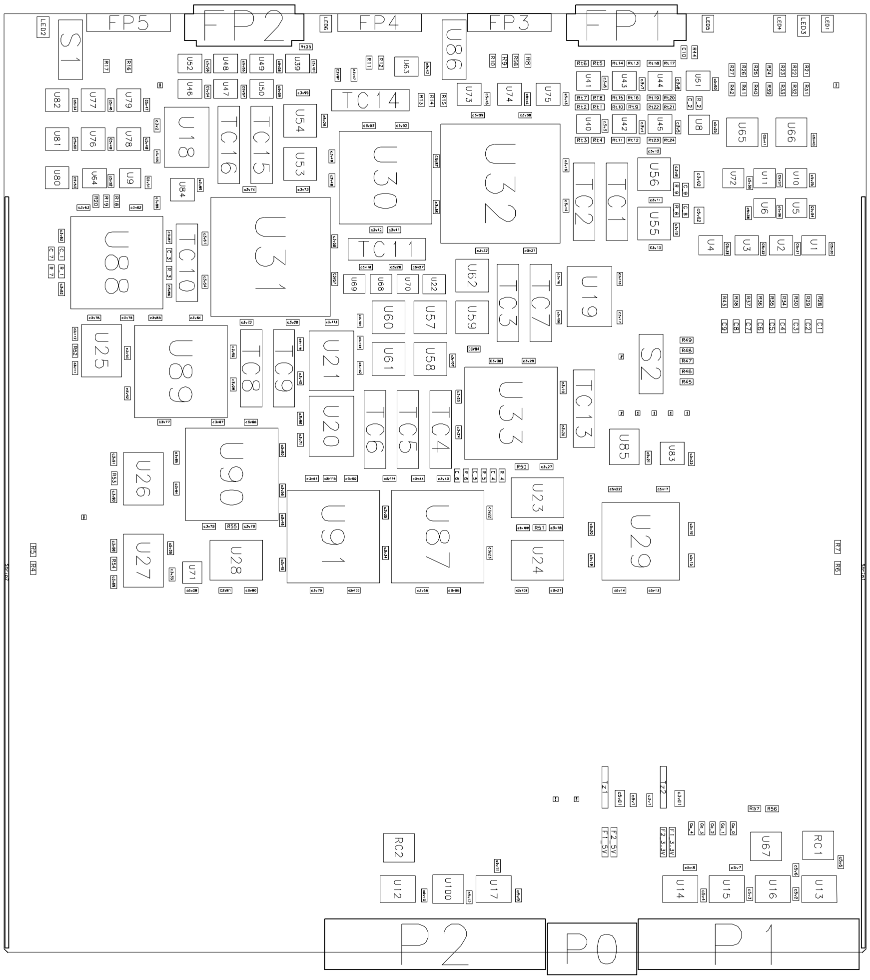


Figure 14: The Track Fitter board layout

TF parts list v1.2 (Jan 28/99)

Purpose	Vendor	Part Number	Description	Package	#order	#/board	$/unit	$/board	comments	When?	in the scematics
FEP & OPP	Altera	EPF10K100ABC600-1	FPGA	BGA 600		2	495	990			1(FEP/PROCESSOR), 1(OPP)
FIT/CONTROL	Altera	EPF10K50VBC356-3	FPGA	BGA 356		1	119	119	may be replaced by EPF10K30ABC356-3		1(FITTER/CNTRL)
FIT/PROCESSOR	Altera	EPF10K100ABC356-1	FPGA	BGA 356		6	398	2388			6(FITTER/FIT)
VME Interface	Altera	EPM7128SQC160-7	CPLD	PQDP 160		1	40	40			
HB-FIFO	Cypress	CY7C4245V-15ASC	FIFO 4kx18	A64(10x10 TQFP64)	5	2	43.4	86.8			2(FP/DATAIN)
TF-FIFO	Cypress	CY7C4215V-15ASC	FIFO 512x18	A64(10x10 TQFP64)	14	6	27.3	163.8		12/23	
BP-FIFO	Cypress	CY7C4285V-25ASC	FIFO 64kx18	A64(10x10 TQFP64)	6	2					2(OPP/BP_FIFO)
ISPY & OSPY	Motorola	MCM69F737TQ8	BurstRAM 128kx36	TQFP	5	2	51.49	102.98		12/23	1(FEP/ISPY), 1(OPP)
Memory Lookups	Motorola	MCM69F536CTQ10	BurstRAM 32kx36	TQFP	5	2	15.2	30.4	10 nsec		2(FITTER/CNTRL)
Flash Memory	Intel	DT28F160S3-100	FlashFile Memory 1Mx16	SSOP56	14	6	11.95	71.7	NoCommercial temp. range device?	12/23	6(FITTER/FIT)
LVDS Drivers	National	DS90LV031ATM	quad LVDS driver	SOP/M16A	18	7	7.65	53.55		12/23	1(FP/DATAIN), 6(FP/DATAOUT)
LVDS Receivers	National	DS90LV032ATM	quad LVDS receiver	SOP/M16A	18	7	7.65	53.55		12/23	6(FP/DATAIN), 1(FP/DATAOUT)
VME Receivers	IDT	74FCT541ASO	Octal buffer/receiver	SOIC 20	10	4	1.32	5.28		12/23	4(TF_VME/VME)
VME Transceivers	TI	SN74ABTE16245DL	16 bit transceiver	SOIC 48	15	6	6	36			6(TF_VME/VME)
VME o/c buffer	TI	SN74BCT760DW	Octal O/C buffer	SOIC 20	6	2	2.5	5		12/23	1(TF_VME/VME), 1(TF_VME/VME/P2)
Clock Driver	ITD	IDT74FCT3807AQ	1-TO-10 clock driver	QSOP20	3	1	5.83	5.83			1(OPP)
LED Driver	TI	SN74BCT760DW	Octal Buffers/drivers	SOIC20	10	4	2.5	10		12/23	Front_Panel/LED
4BIT 1/2 Multiplexer	TI	SN74CBT3257	4 Bit 1/2 Multiplexer	SOIC16	6	2	1.37	2.74	w/ EPC1	12/23	FP/CONFIG
Monostabel vibrator	Philips	74HCT123D	Dual monostable vibrator	soic16	20	8	0.41	3.28		12/23	Front_Panel/LED
NAND Gate	Philips	74HCT00D	Quad NAND Gate	SOIC14	3	1	0.29	0.29		12/23	1 (FP/LED), 1(FP/DATAIN), 1(FP/DATAOUT)
NOR Gate	Philips	74HCT02D	Quad NOR Gate	SOIC14	3	1	0.29	0.29		12/23	2(FP/LED)
AND Gate	TI	SN74AS08D	Quad AND Gate	SOIC14	3	1					1(FP/LED)
AND Gate	Philips	74HCT08D	Quad AND Gate	SOIC14	6	2	0.19	0.38			5(FP/LED),
OR Gate	TI	SN74AS32D	Quad OR Gate	SOIC14	3	1	0.57	0.57		12/23	2(FP/DATAIN)
Invertor	TI	SN74AS04D	Hex Invortor	soic14	6	2	0.57	1.14		12/23	1(FP/LED), 1(TF_VME)
10MHz oscillator	digkey	SG-531P-10.0000MC	CMOS/TTL	dip8	2	(1)	3	0		12/23	
25 MHz Oscillator	digkey	SG-531P-25.0000MC	CMOS/TTL	dip8	2	(1)	3	0			
30 MHz Oscilator	digkey	SG-531PTJ-30.000MC	TTL	dip8	3	1	3	3		12/23	
33 MHz Oscillator	digkey	SG-531PTJ-33.000MC	TTL	dip8	2	(1)	3	0		12/23	
36 MHz Oscillator	digkey	SG-531PTJ-36.000MC	TTL	dip8	2	(1)	3	0		12/23	
40 MHz Oscillator	digkey	SG-531PH-40.000MC	CMOS	dip8	2	(1)	3	0		12/23	
Osillator socket	digkey	A463-ND	socket	dip8	3	1	0.53	0.53		12/23	
EPC1	ALTERA	EPC1PC8	PROM	dip8	25	10	7.3	73		12/23	FP/CONFIG
EPC2	ALTERA	EPC2		20-pin PLCC	20	7					FP/CONFIG
dip8 socket			dip8 socket		25	10				12/23	FP/CONFIG
10 nsec delay	DDD	3D7304D-10	4 delay Units	SOIC14	3	1	17.25	17.25	DDD = Data Delay Devices	12/23	1(OPP), 3(TF_VME/VME)
15 nsec delay	DDD	3D7304D-15	4 delay Units	SOIC14	3	1	17.25	17.25		12/23	4(OPP)
40 nsec delay	DDD	3D7304D-40	4 delay Units	SOIC14	5	2	17.25	34.5		12/23	see delay.txt
40nsec tap delay	DDD	SMD99F-5200	5 tap delay		3	1	14	14		12/23	1(TF_VME)
3 Color(GYR) LED	MENTOR	1802.2781	Green/Yellow/Red		6	2			SVT Bottom LED & TF Special (middle?)		Front_Panel/LED
2 Color(RY) LED	MENTOR	1801.2731	Yellow/Red		3	1			SVT Top LED		Front_Panel/LED
2 Color(GR) LED	MENTOR	???	Green/Red		6	2			LED on the connector (IN/OUT)		Front_Panel/LED
2 Color(RR) LED	MENTOR	???	Red/Red		3	1			TF Special LED for the EPROM1x2		Front_Panel/LED
390 Ohm Register						2					2(TF_VME/VME)
1k Registor						21			w/ LED , w/ EPC1, w/SVT Data		10(FP/LED), 10(FP/CONFIG), 1(FP/DATAIN)
10k Register						3			w/ VME bit blaster		3(FP/CONFIG),
100k Registor						8			w/ 74HCT123		
470 pF									for the SVT data line		1(FP/DATAIN),
2uF Capacitor						8			w/ 74HCT123		
SVT Input connector	KEL	8822E-052-171H	52 bits connector			2			SVT connectors for INPUT and OUTPUTs		FP/(DATAIN, DATAOUT)
Bit Blaster Connector						3					FP/CONFIG
2 dip switch						1			w/ EPC1		FP/CONFIG
Total $ of parts/board											
4330.11											

Figure 15: The Track Fitter parts list

delay module, and TTL gates use 5V. Therefore, there are two fuses, one each for 3.3V and 5V. All of the 3.3V ALTERA FLEX chips have a global output enable line connected to 5V. Therefore, if 5V fails, the chip output goes to a tri-state condition, protecting all of the 5V chips from a 3.3V signal input. If 3.3V fails, the ALTERA chip is tolerant to 5V. All other 3.3V components are connected to an ALTERA chip, and they are safe. We use 5V FIFOs for the INPUT FIFOs since they communicate with 5V LVDS receivers and some TTL gates.

When we are ready to build pre-production modules, we will consider changing all 5V components to 3.3V versions if they are available.

C Some Remarks on the Proto-type

For the BP_FIFO, we planned to use a CY7C4285V (64k $\times$ 18), but actually used a CY7C4245V (4k $\times$ 18). CY7C4285V is NOT tolerant to 5V, but its write-clk is connected to the output of the 5V delay module. Therefore, temporarily we are using CY7C4245V, which is tolerant to 5V. For the pre-production module, the design will be fixed.