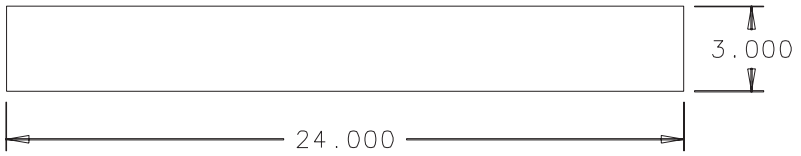
A2696 BOARD SPECIFICATIONS

A2696 BOARD DIMENSION (Inch)



BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.038	768	YES	---
⊞	.041	4	YES	---
⌀	.065	48	YES	---
⊟	.128	16	YES	---
⊖	.15	9	YES	---

1. Board Layers: 10
2. Layer Stack Order:
   * Layer1 (Artwork_1): Top component layer, Filled with solid ground 0.5oz
   Layer2 (Artwork_2): signal_3, 0.5oz, Z(diff)=100ohm
   Layer3 (Artwork_3): Ground, Drawing_1, 1oz
   Layer4 (Artwork_4): signal_4, 0.5oz, Z(diff)=100ohm
   Layer5 (Artwork_5): Ground, drawing_2 1oz
   Layer6 (Artwork_3): Ground, Drawing_1 1oz
   Layer7 (Artwork_6): signal_5, 0.5oz, Z(diff)=100ohm
   Layer8 (Artwork_5): Ground, drawing_2 1oz
   Layer9 (Artwork_7): signal_6, 0.5oz, Z(diff)=100ohm
   * Layer10 (Artwork_8): Bottom component layer, Filled with solid ground, 0.5oz
3. Apply silkscreen on both Top and Bottom component side:
   Artwork_9: Top silkscreen.
   Artwork_10: Bottom silkscreen.
4. Apply solder mask over bare copper on both side:
   Artwork_11: two layers epoxy(2-3u) top solder mask
   Artwork_12: two layers expoxy (2-3u) bottom solder mask
5. Material: FR4
6. Board thickness: 0.120'' +/- 0.010.
7. Minimum Diff. Trace/gap/trace= 7/5/7 mils
8. Trace impedance control: 100 ohms +/-10% for all diffrential 7/5/7 pairs
9. Board finish type: IM-TIN
10. All dimensions are in inches unless otherwise noted.

* Please note top and bottom layer are also ground planes

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SPC# A2696
ASM# A2697

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
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SHEET 1 OF 1
DATE 06/01/2010
DRAWN LIN

B- 2696
REV 1.0