4-channel sampling chip design

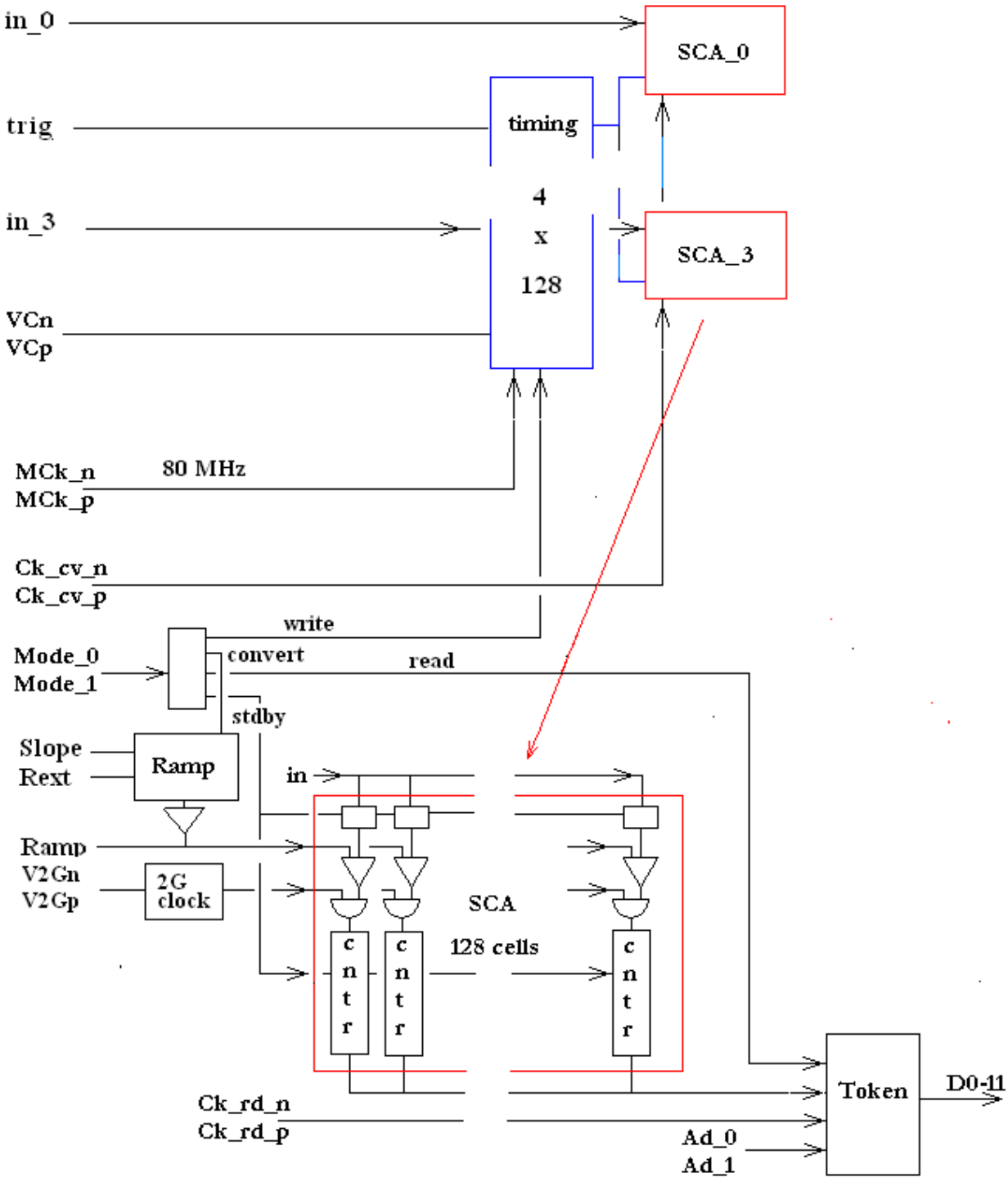
Overview, Architecture.

Use a switched capacitor array (SCA) as an analog memory clocked with a fast timing generator to record the history from a detector output.

First chip is a demonstrator: the goal is to obtain a timing resolution of a few picoseconds from fast MCP detectors after pulse reconstruction.

Design options:

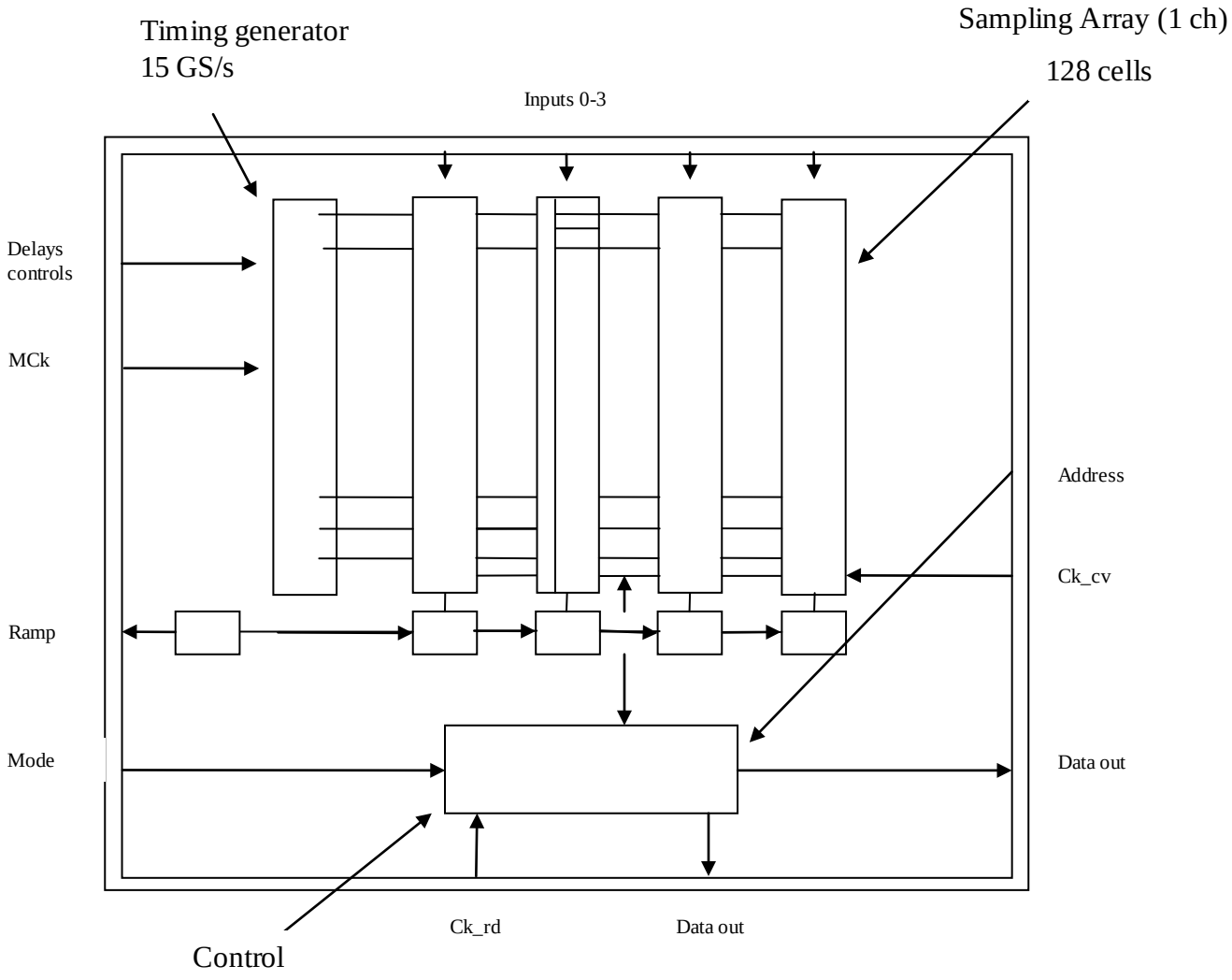
15 GS/s sampling
1.5 GHz analog bandwidth
128 cells (5-10ns recording time)
No PLL (to be implemented later)
4-channel
12-bit ADC
130nm CMOS technology


in_0
SCA_0
trig
timing
4
x
128
in_3
SCA_3
VCn
VCp
MCk_n
MCk_p
80 MHz
Ck_cv_n
Ck_cv_p
write
Mode_0
Mode_1
convert
read
stdby
Slope
Rext
Ramp
in
Ramp
V2Gn
V2Gp
2G
clock
SCA
128 cells
cntr
cntr
cntr
Token
D0-11
Ck_rd_n
Ck_rd_p
Ad_0
Ad_1

Pad Name	Type	Signal	Function
In_1-4	a I		Analog inputs 0 -1.2V
Trig	a I		Trigger 0 -1.2V Stops the recording process
MCk_n MCk_p	d I	diff	Write clock (80 MHz to timing generator)
Ck_cv_n Ck_cv_p	dO	diff	ADC clock output (2 GHz/4096=500 kHz)
Ck_rd_n Ck_rd_p	d I	diff	Read clock (50 MHz)
VCN	aI		Controls delay of timing cell (falling)
VCP	aI		(rising)
V2GN V2GP	aI aI		Controls 2G counter ring oscillator
Ramp_n Ramp_p	a IO	diff	External ramp input, or internal ramp output
Mode_0-1	d I		00 write writes continuously samples of inputs in a caps arrays at 15 GS/s for 6.4us. Sampling stopped upon trigger 01 convert starts ramp and counters at 2 GHz for 2 us 10 read sequences 128 counters outputs onto data bus at 50 MHz 11 stand-by clear sampling caps, reset counters
AD0-1			Channel address selects channel for read
D0-11	d I	3_state bus	12-bit data bus
Vdd			+1.2V
Vss			- 1.2V
Gnd			

Gnd	Gnd	In_1	Gnd	Vss	Vdd	Gnd	In_2	Gnd	Vss	Vdd	Gnd	In_3	Gnd	Vss	Vdd	Gnd	In_4	Gnd	Gnd
Vdd																			Vdd
VCN																			AD_0
VCP																			AD_1
Vss																			Vss
Trig																			Gnd
Gnd																			D0
MCk_n																			D1
MCk_p																			D2
Gnd																			D3
Ramp_p																			Vdd
Ramp_n																			Gnd
Ck_rd_n																			Gnd
Ck_rd_p																			Ck_cv_n
Gnd																			Ck_cv_p
Vss																			Gnd
Mode_0																			D4
Mode_1																			D5
Gnd	Vdd	Vss	Vdd	Gnd	Ck_rd_n	Ck_rd_p	Vss	Gnd	D11	D10	Vdd	Gnd	D9	D8	D7	D6	Gnd		

72 pads


Timing generator
15 GS/s
Sampling Array (1 ch)
128 cells
Inputs 0-3
Delays controls
MCk
Address
Ck_cv
Ramp
Mode
Data out
Ck_rd
Data out
Control