Ramp Generator and Super Buffer/Driver Design

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University of Chicago

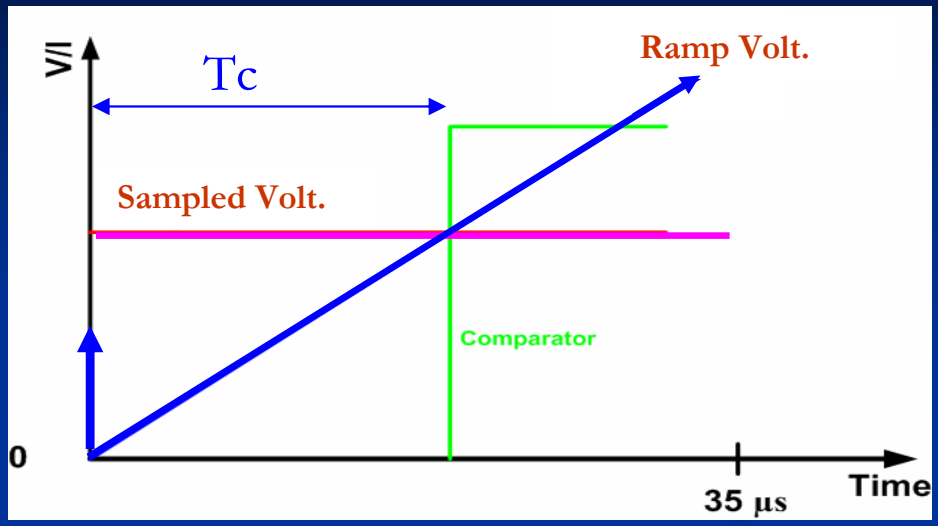
ADC Architecture

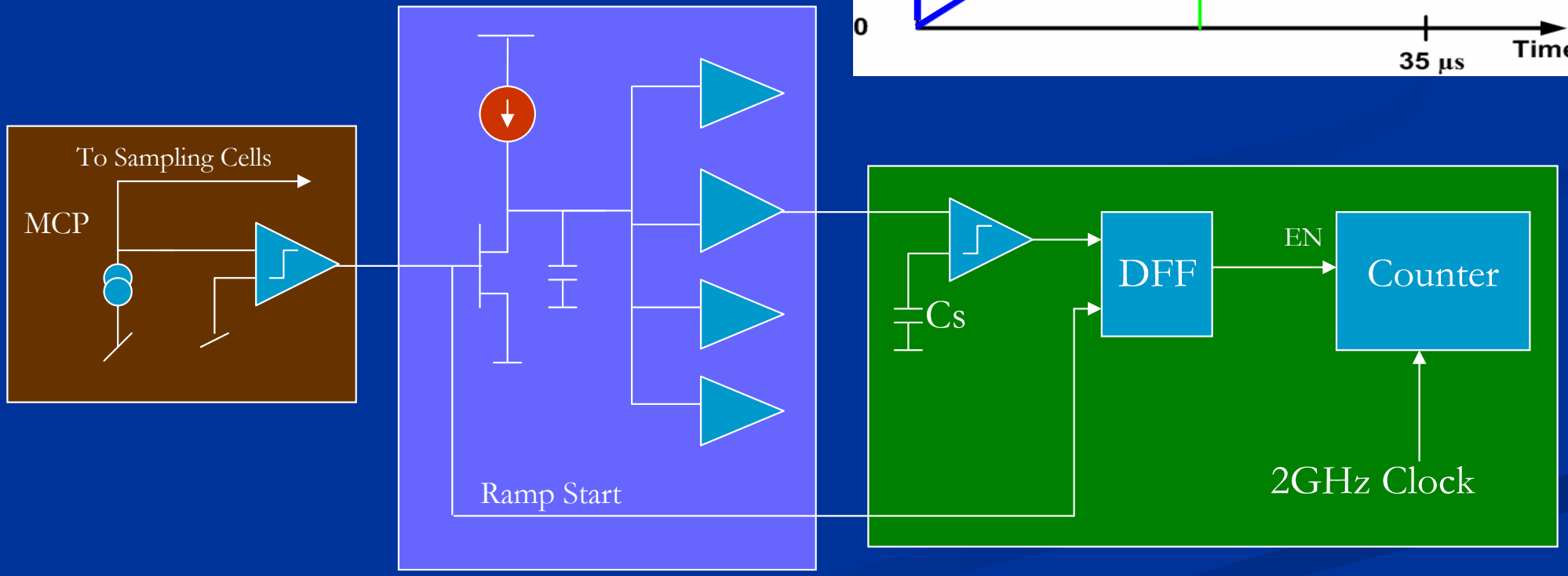
Sampling channel : 4

ADC: 125/Channel

Ramp Gen. : 1

Super Buffer/Driver: 4



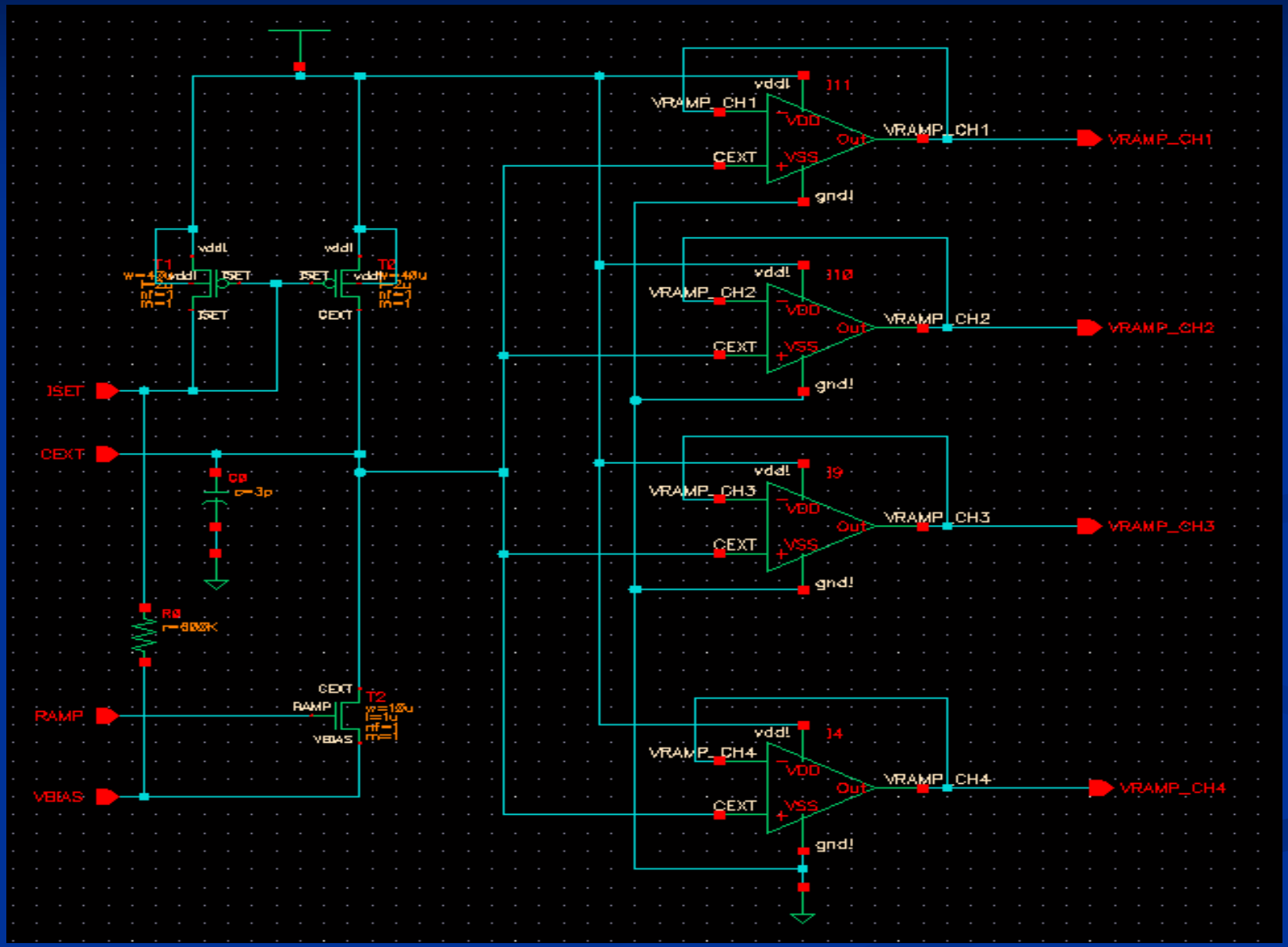


Ramp Gen. & Buffers/Driver

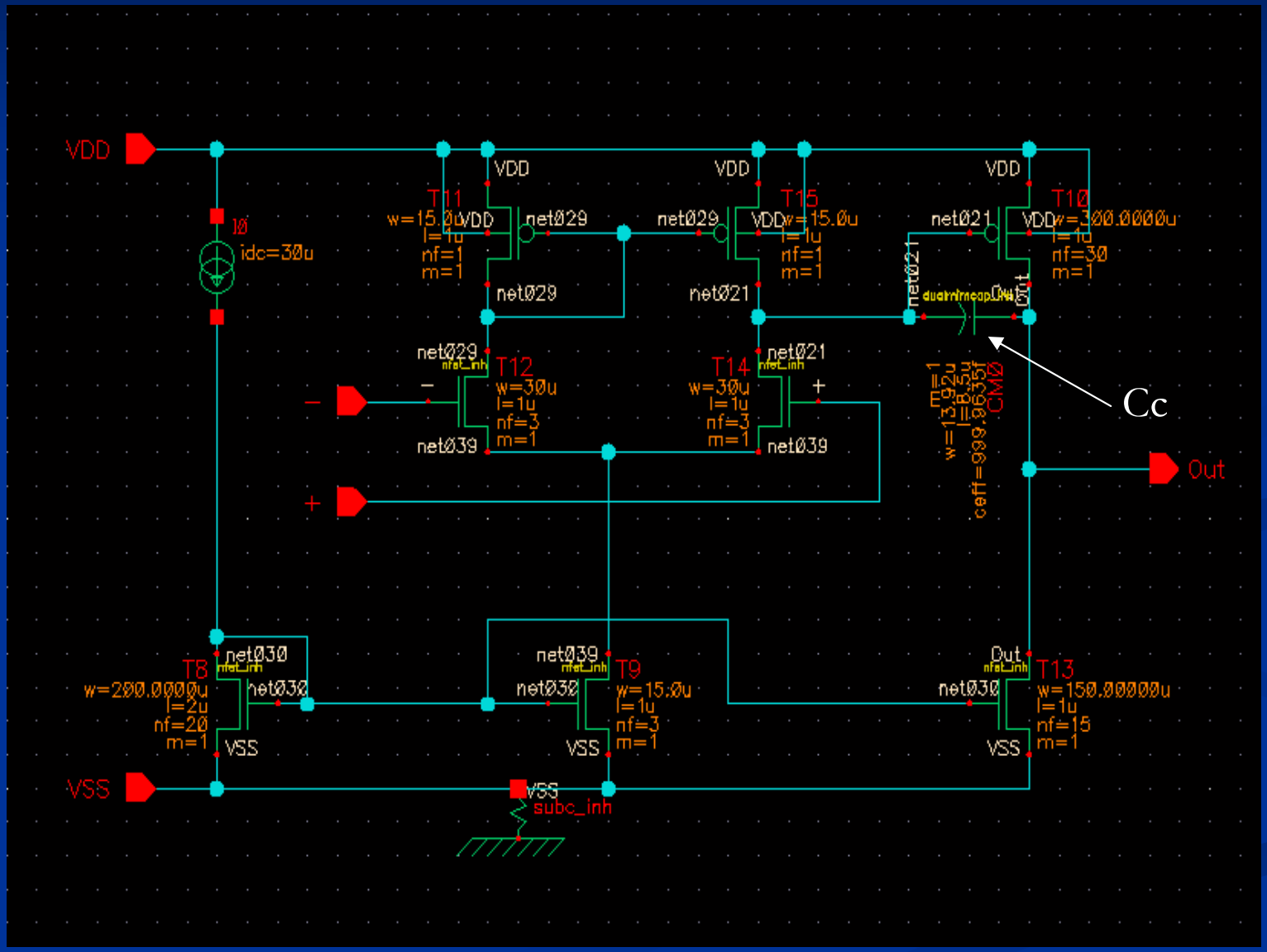
Wilkinson ADC Core

F. Tang

Schematic Diagram of Ramp Generator and Super Buffer/Driver

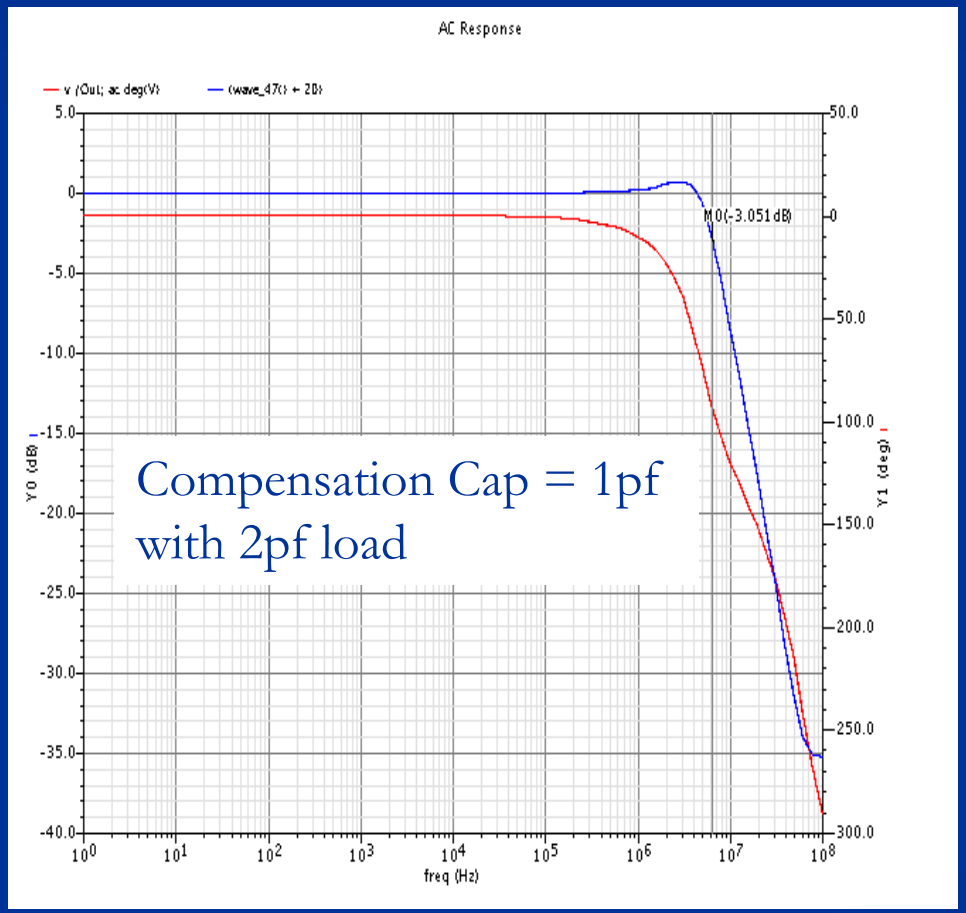


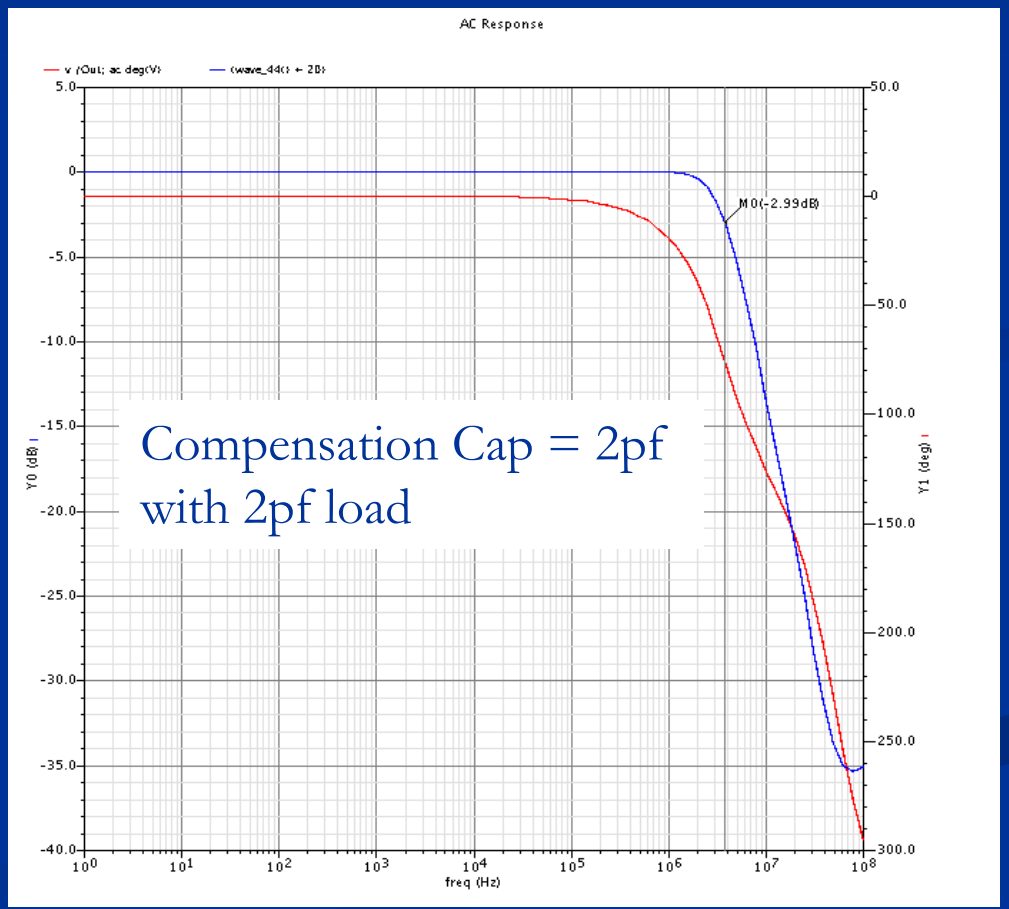
Schematic of Super Buffer/Driver



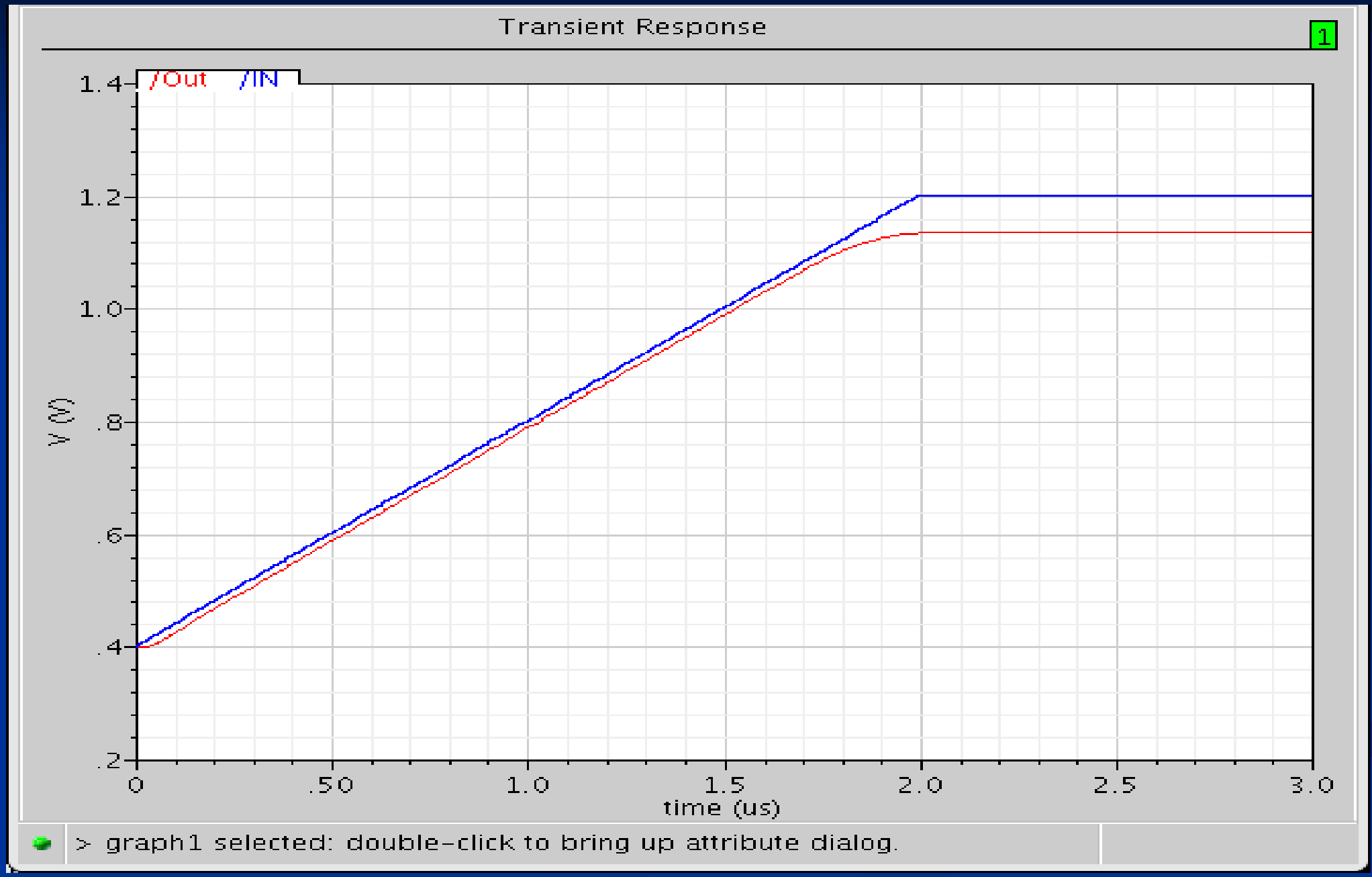
Simulation of Super Buffer/Driver

- Capable to drive 125 comparators (huge load)
- Gian-1 Stable
- Adequate bandwidth (slew rate and noise etc)
- Linearity and dynamic range

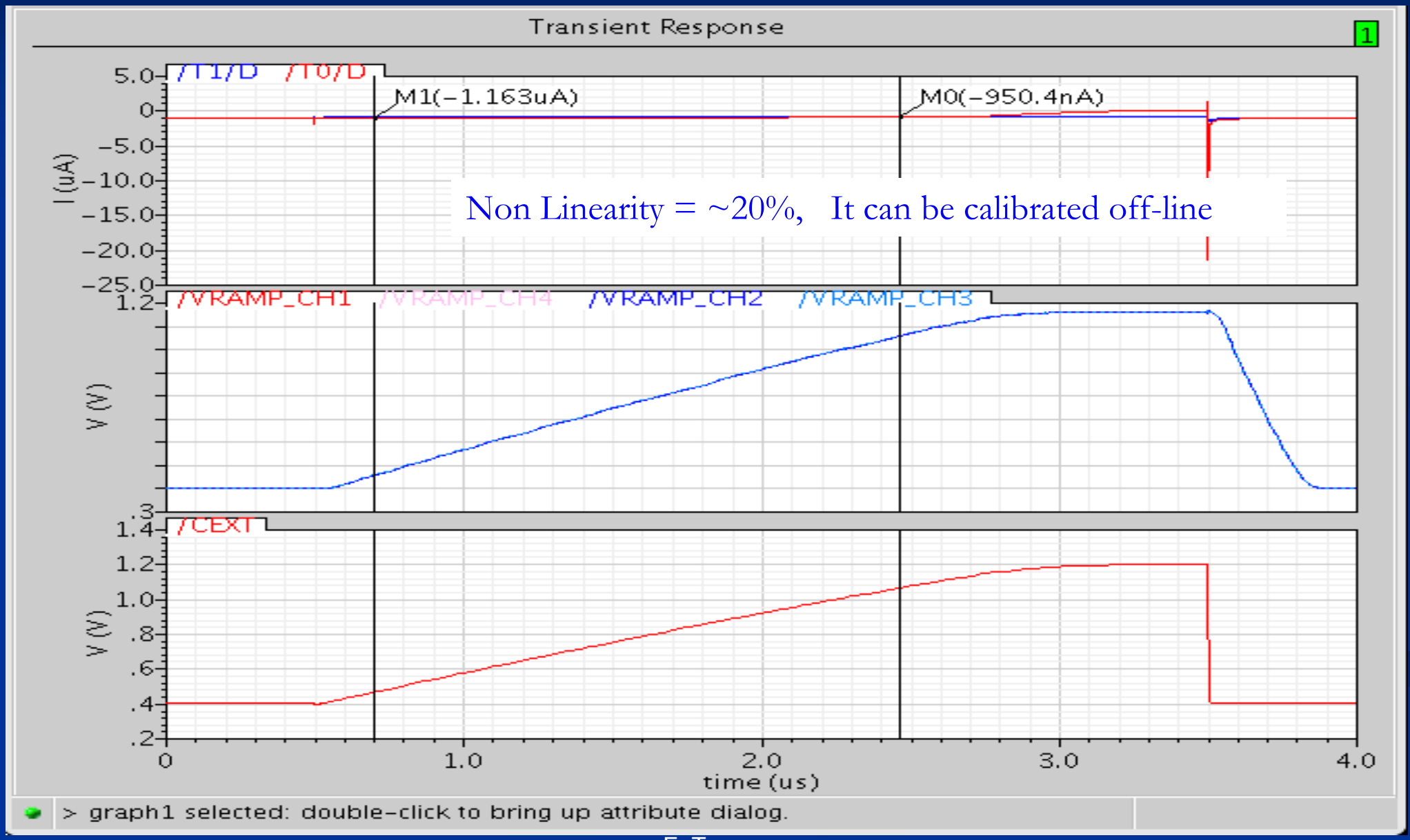




Simulation Results of Super Buffer/Driver



Simulation Results of Ramp Gen. & Super Buffer/Driver



Summary

- Simple current source and low rail voltage presents big non-linearity on ramping current.
- Non-linearity can be calibrated off-line.

Work need to be done:

- Layout
- Post layout simulation
- Minor tuning on gate parameters may be required after post layout simulation

Thank you for your review