Token Controlled Register Readout System

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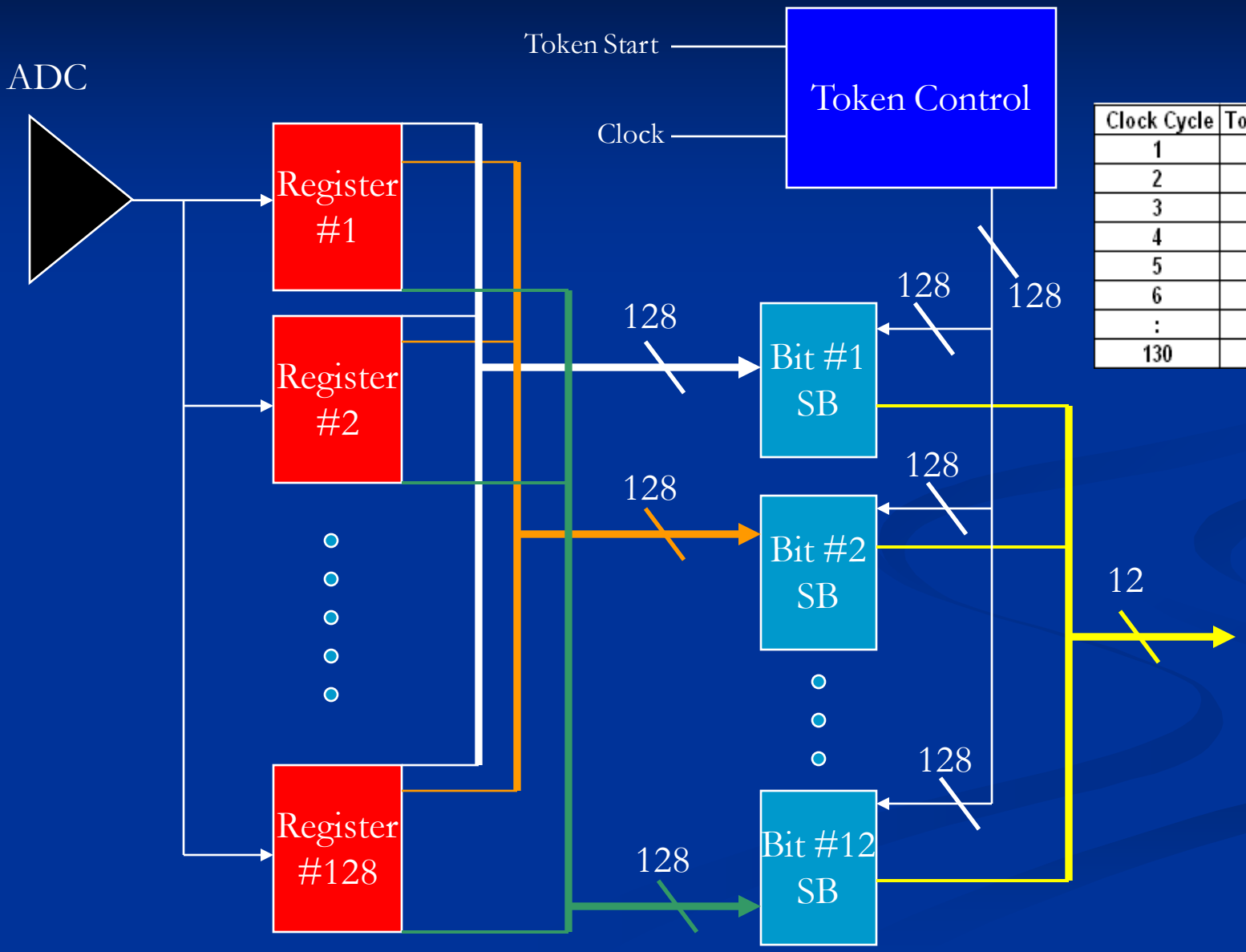
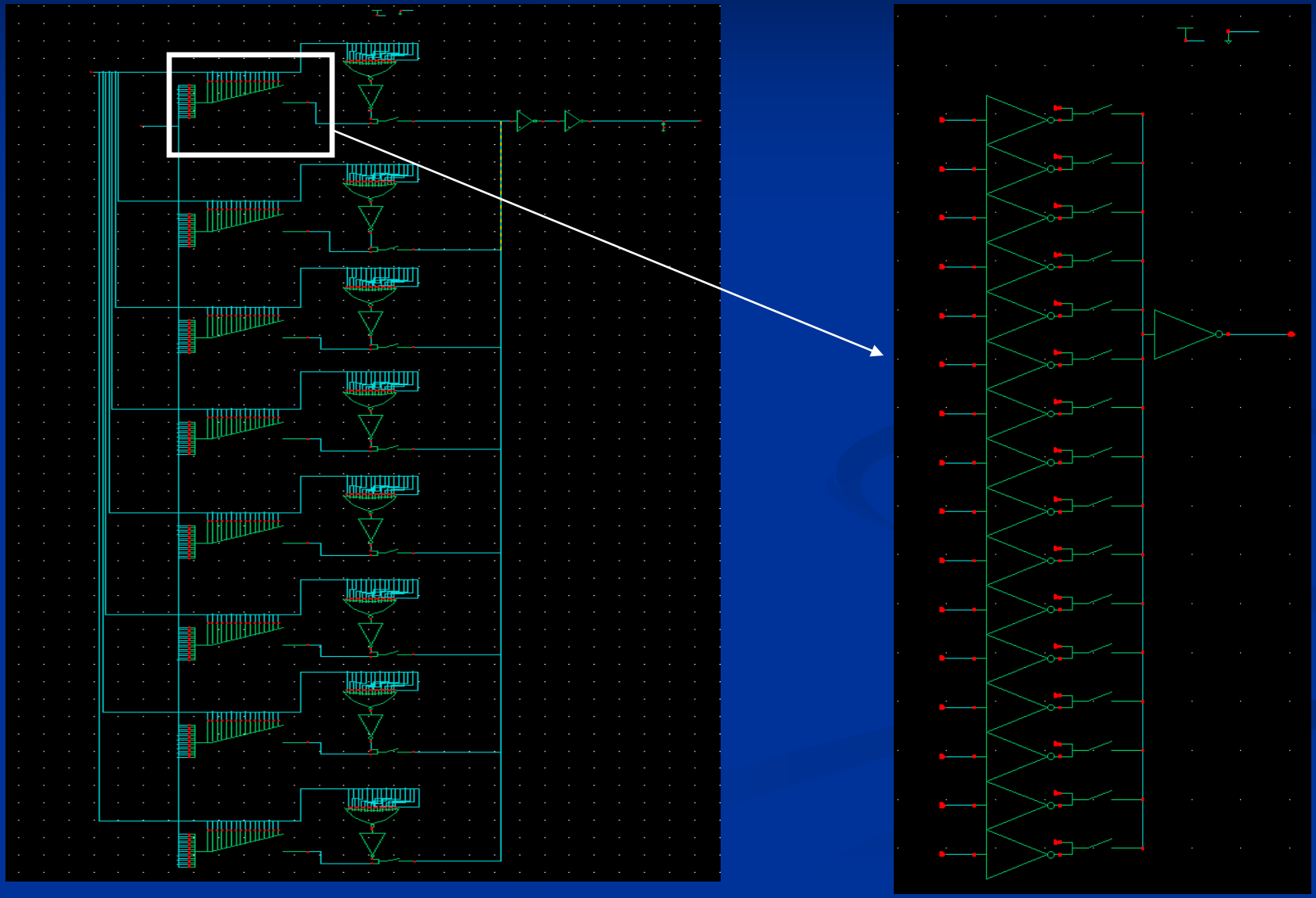
General Idea



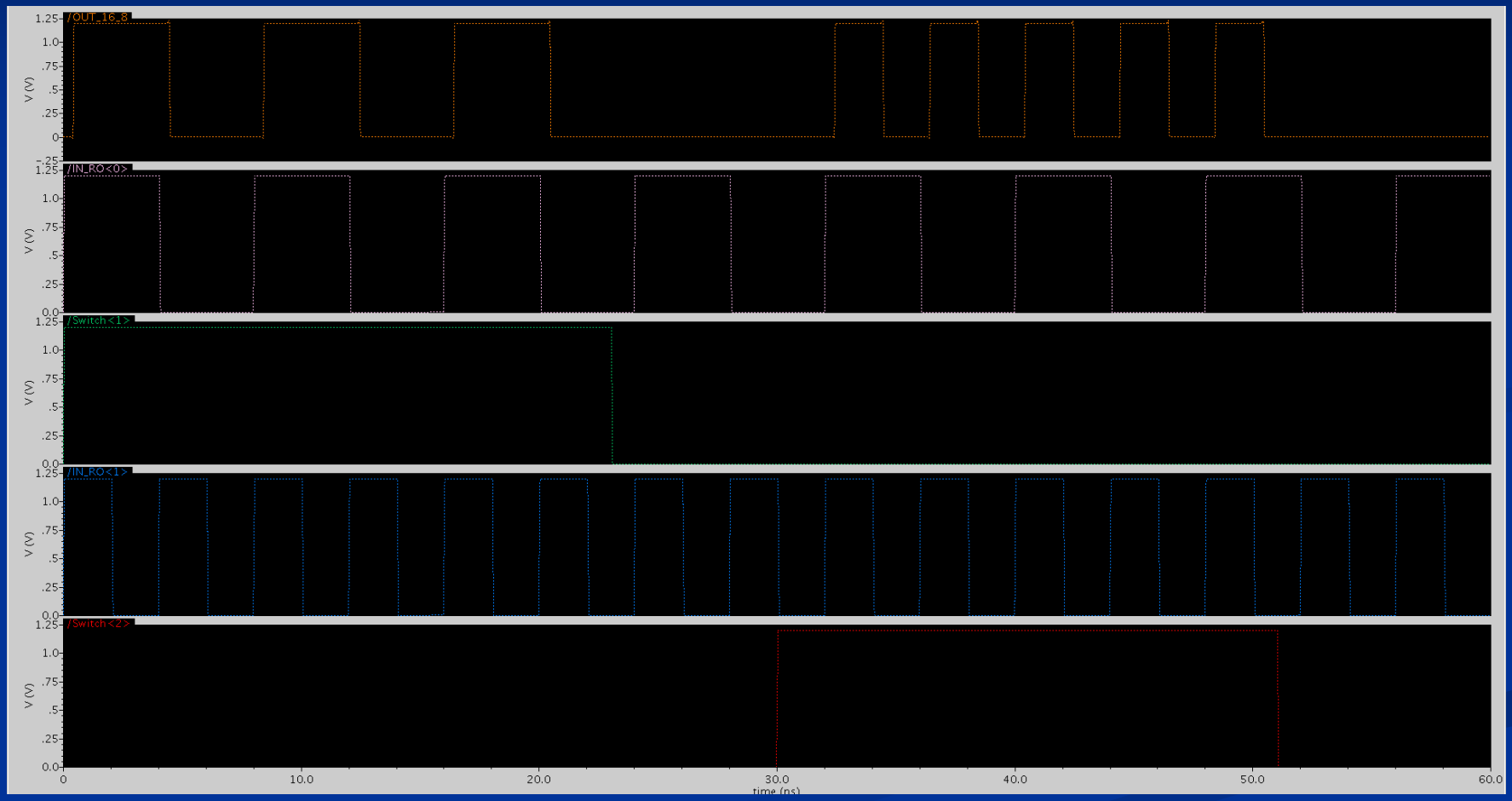
Clock Cycle	Token Start	Bit Switch Active
1	0	none
2	0	none
3	1	1
4	0	2
5	0	3
6	0	4
:	:	:
130	0	128

Bit Switch Box

Stage 1 (16) → Stage 2 (8)

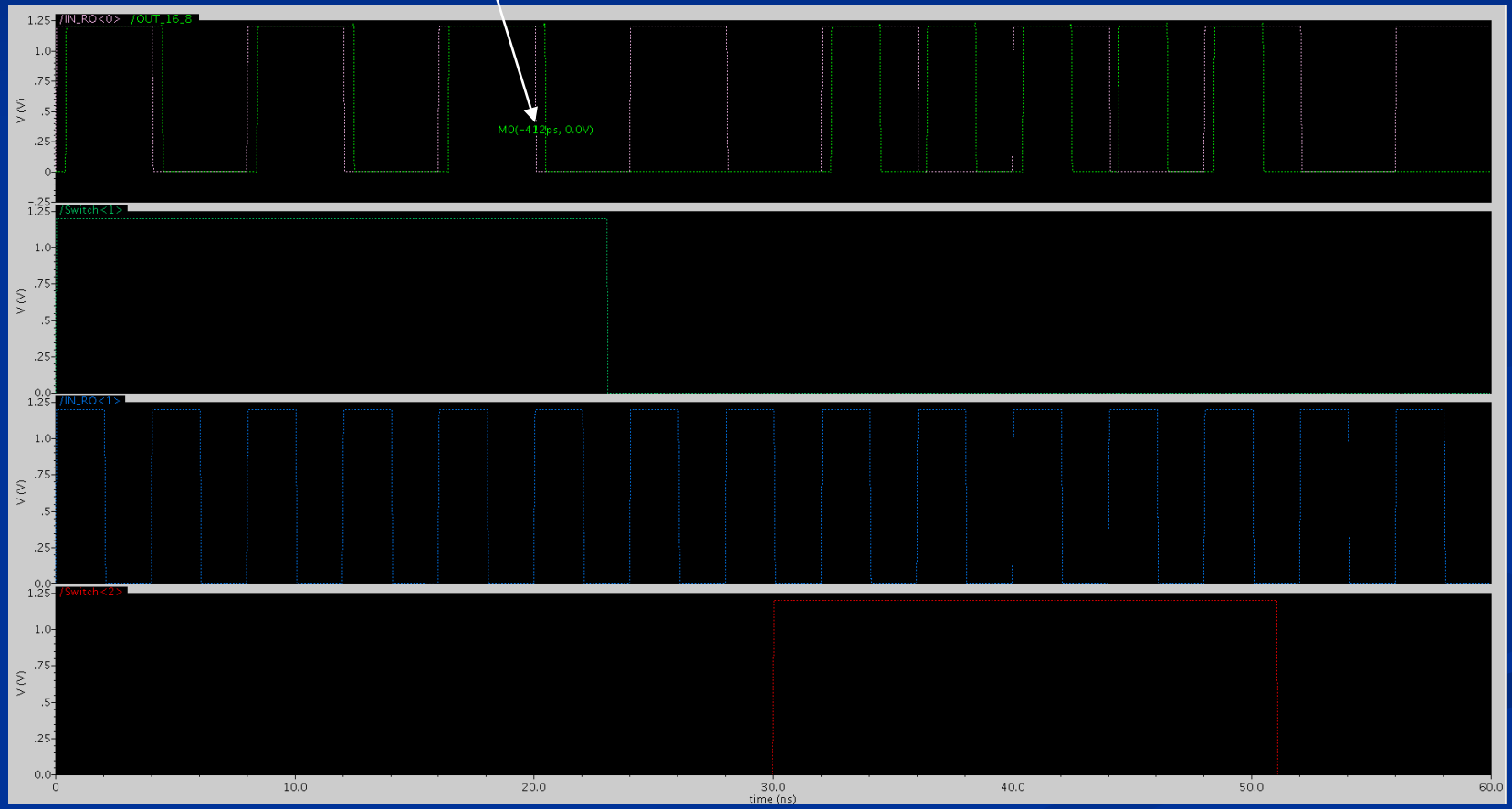


Bit Switch Box

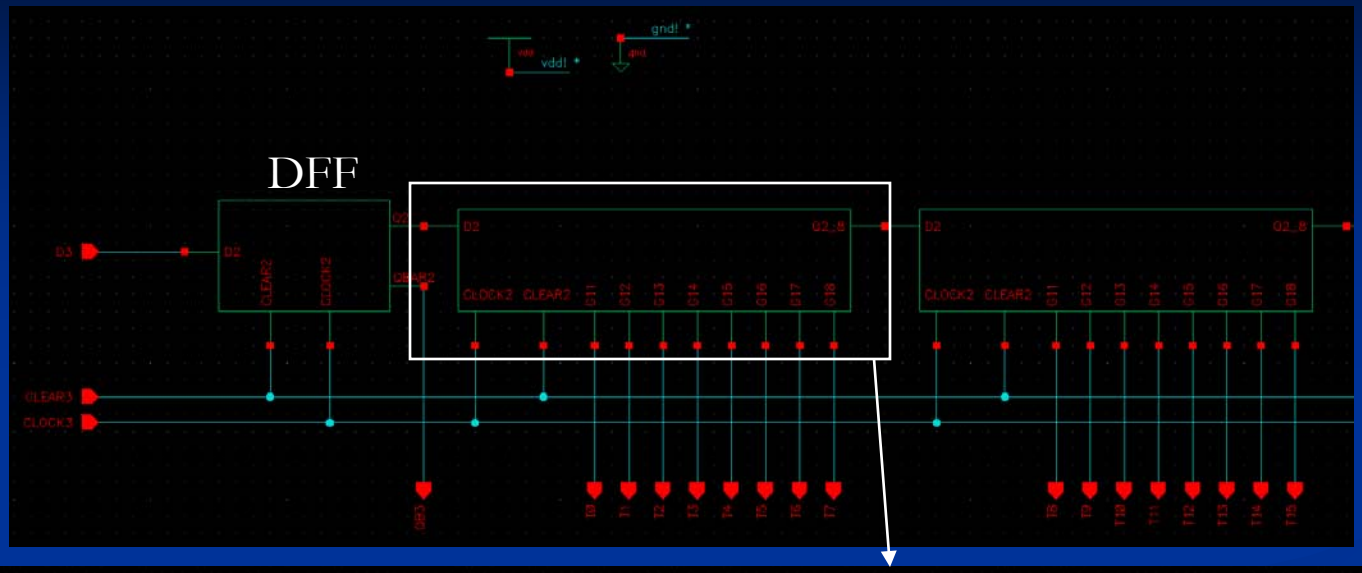


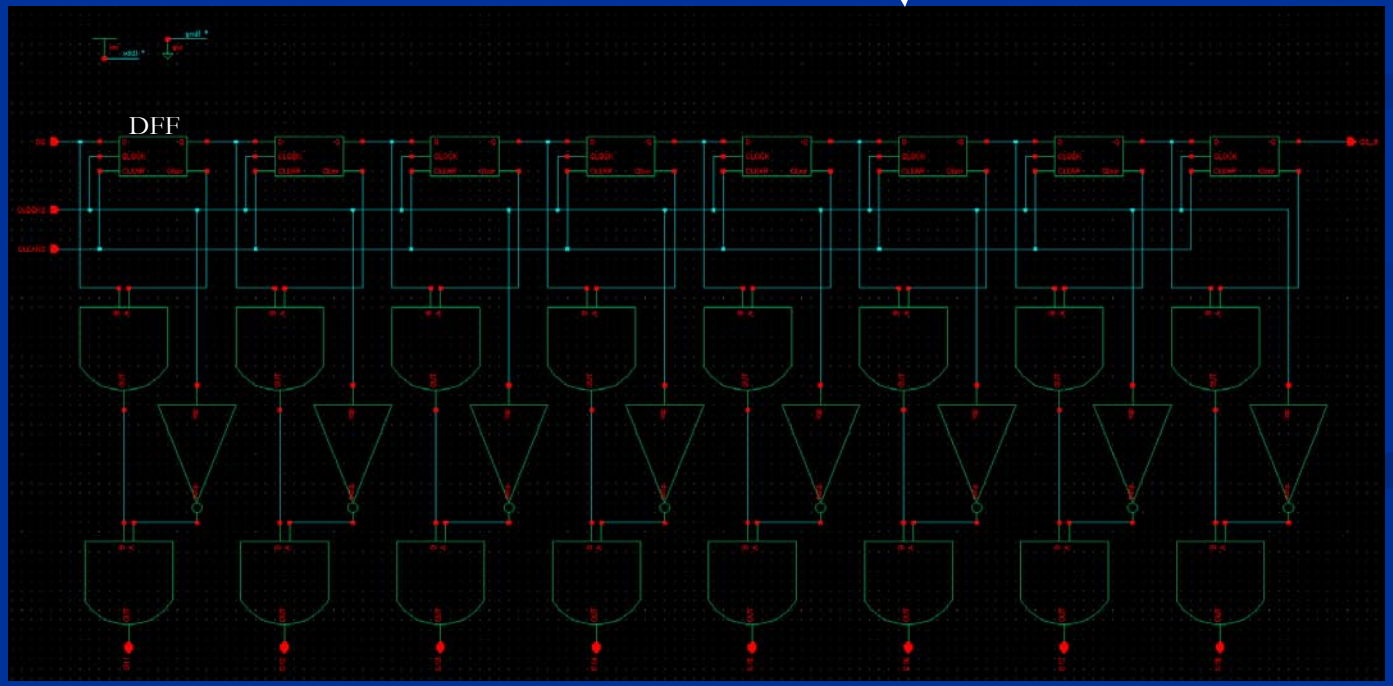
Bit Switch Box

~400ps Delay (no load)

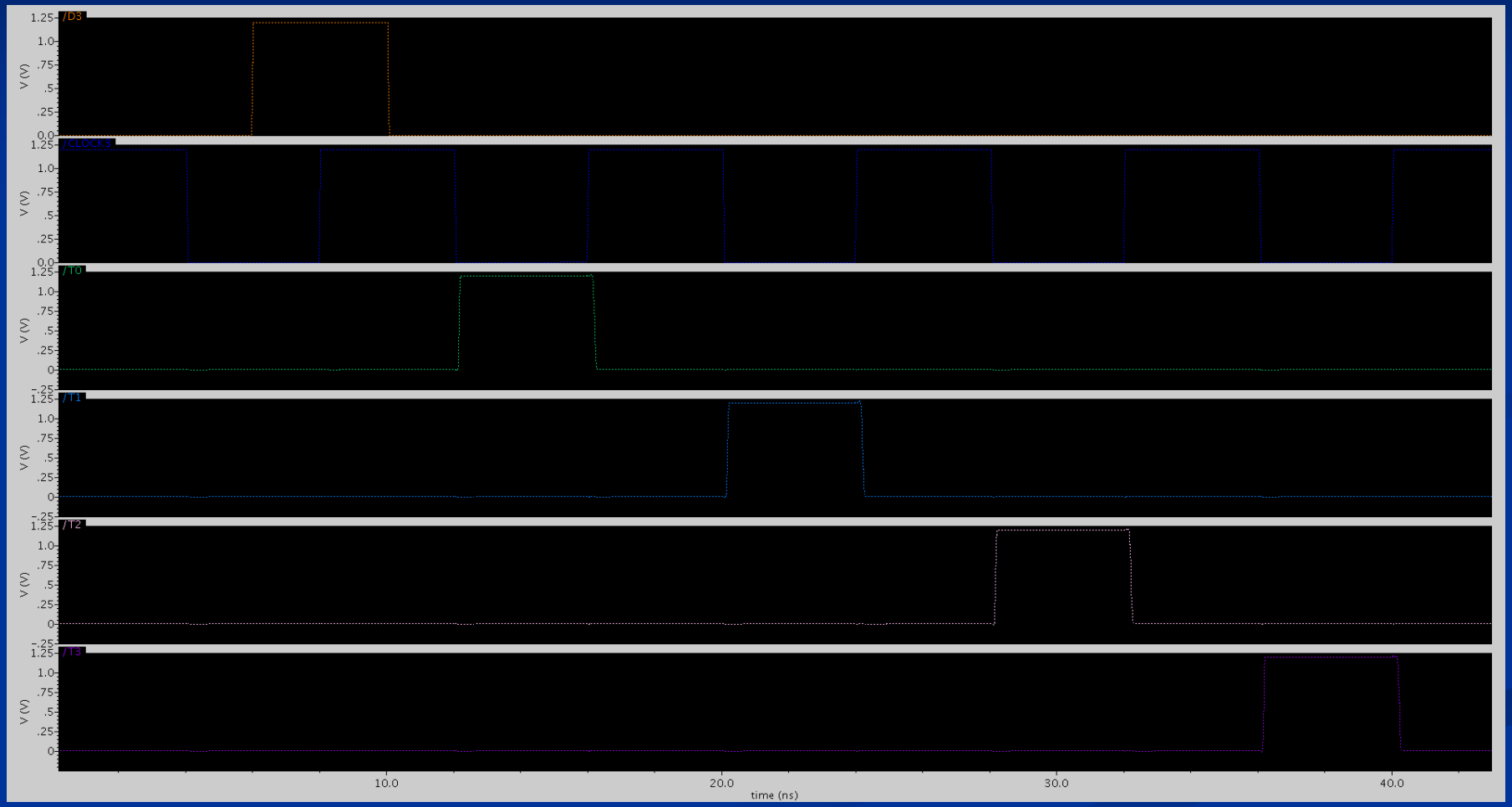


Token Control



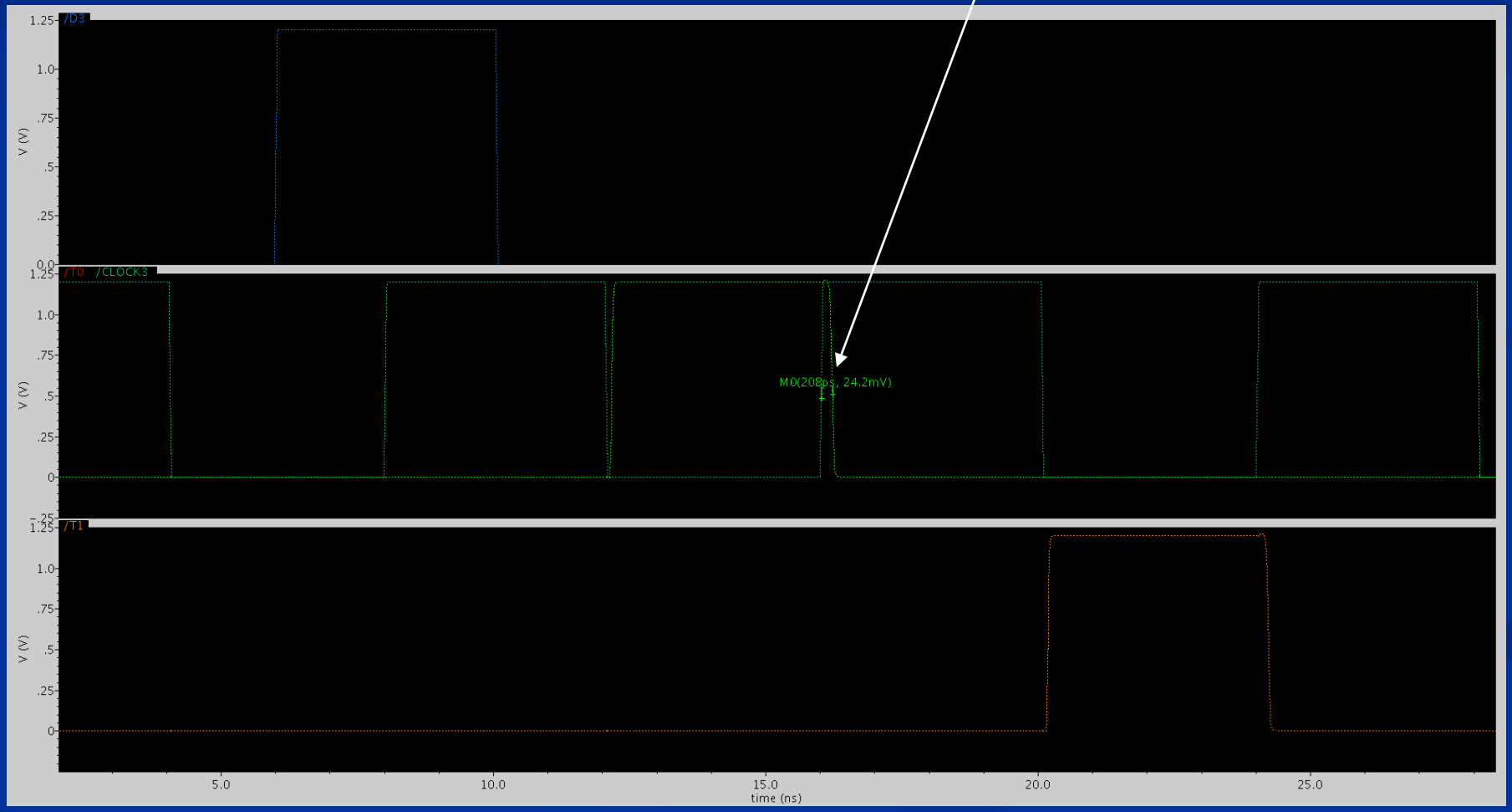


Token Control

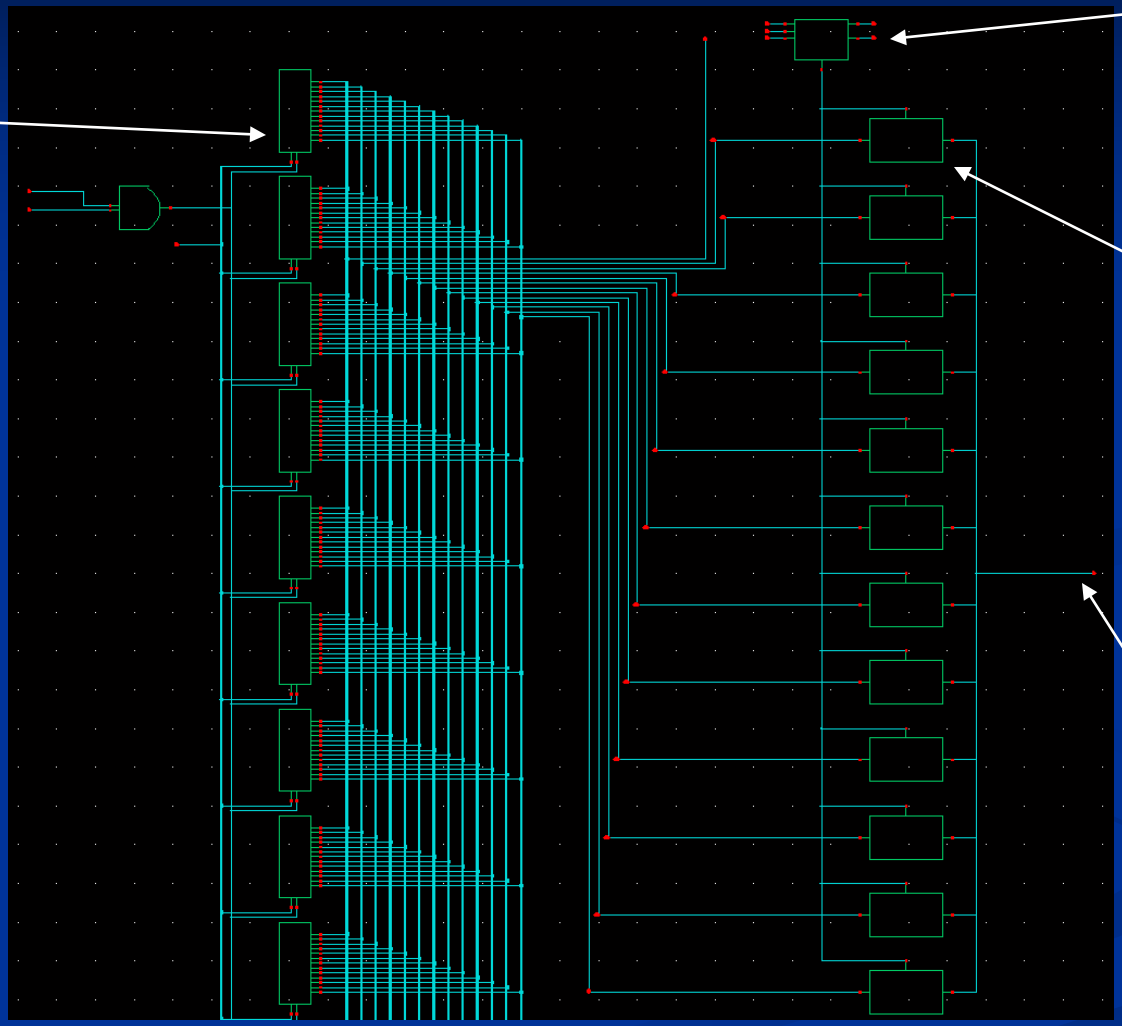
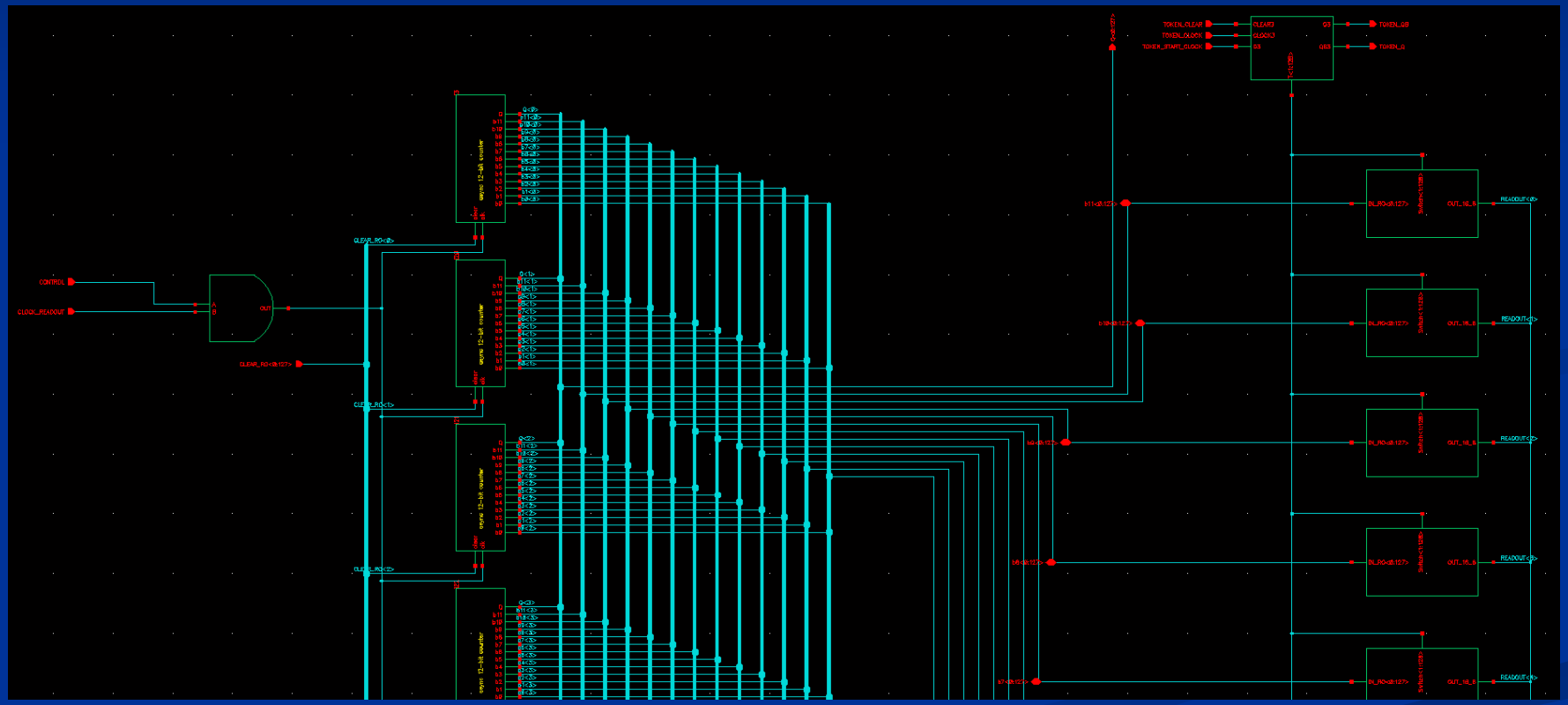


Token Control

~200ps Delay (no load)



Full Readout Schematic



Full Readout Schematic