psASIC Timing Generator

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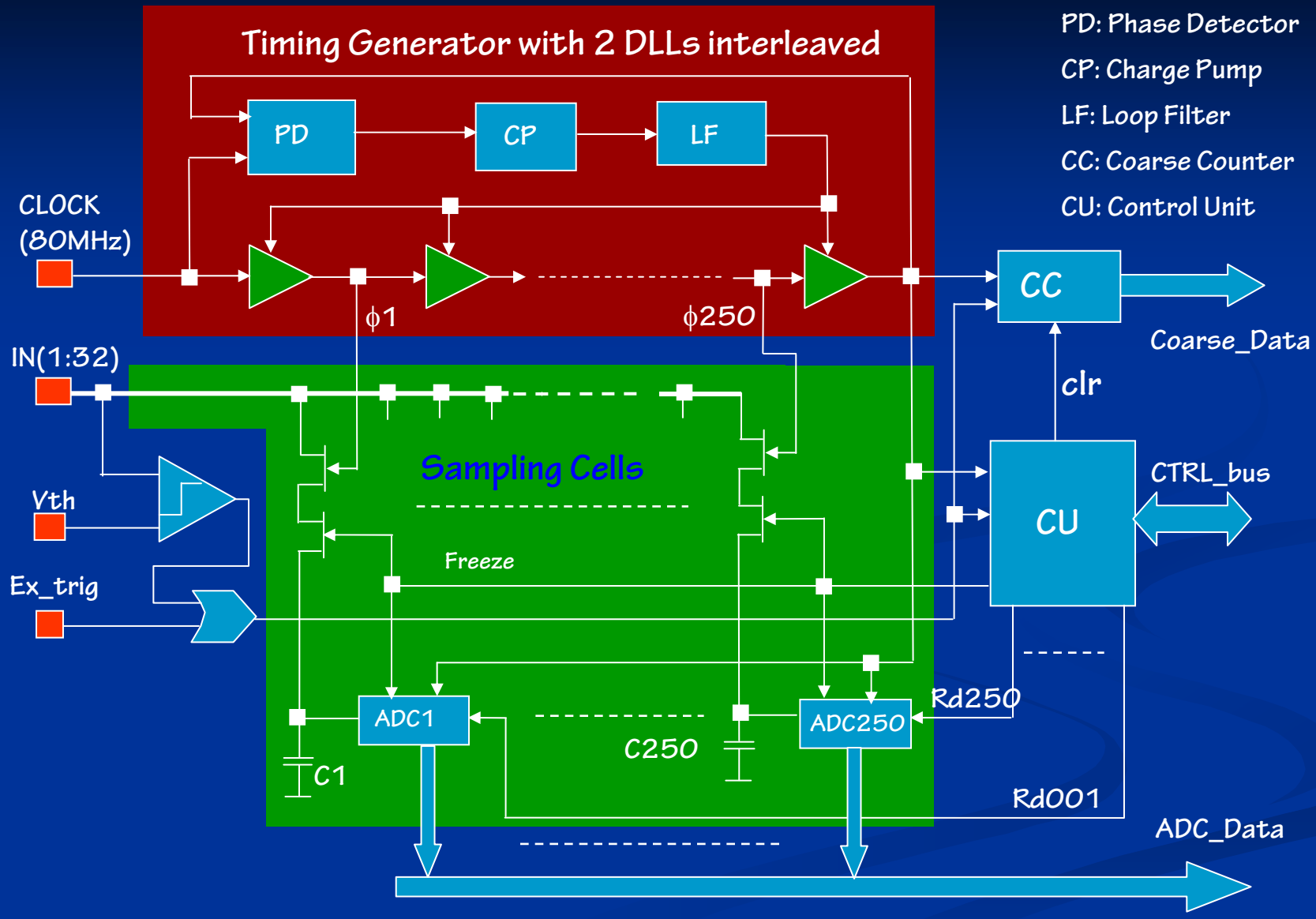
University of Chicago

Diagram of 40Gs/s Sampling Chip



Requirements of Timing Generator

- 80MHz input clock.
- 125 sampling control signals
- 50ps delay time per cell.
- Delay tuning range of delay >10% for DLL in next version.
- 50% duty-cycle (If we can)
- True differential (If we can)
- 1.2V Voltage

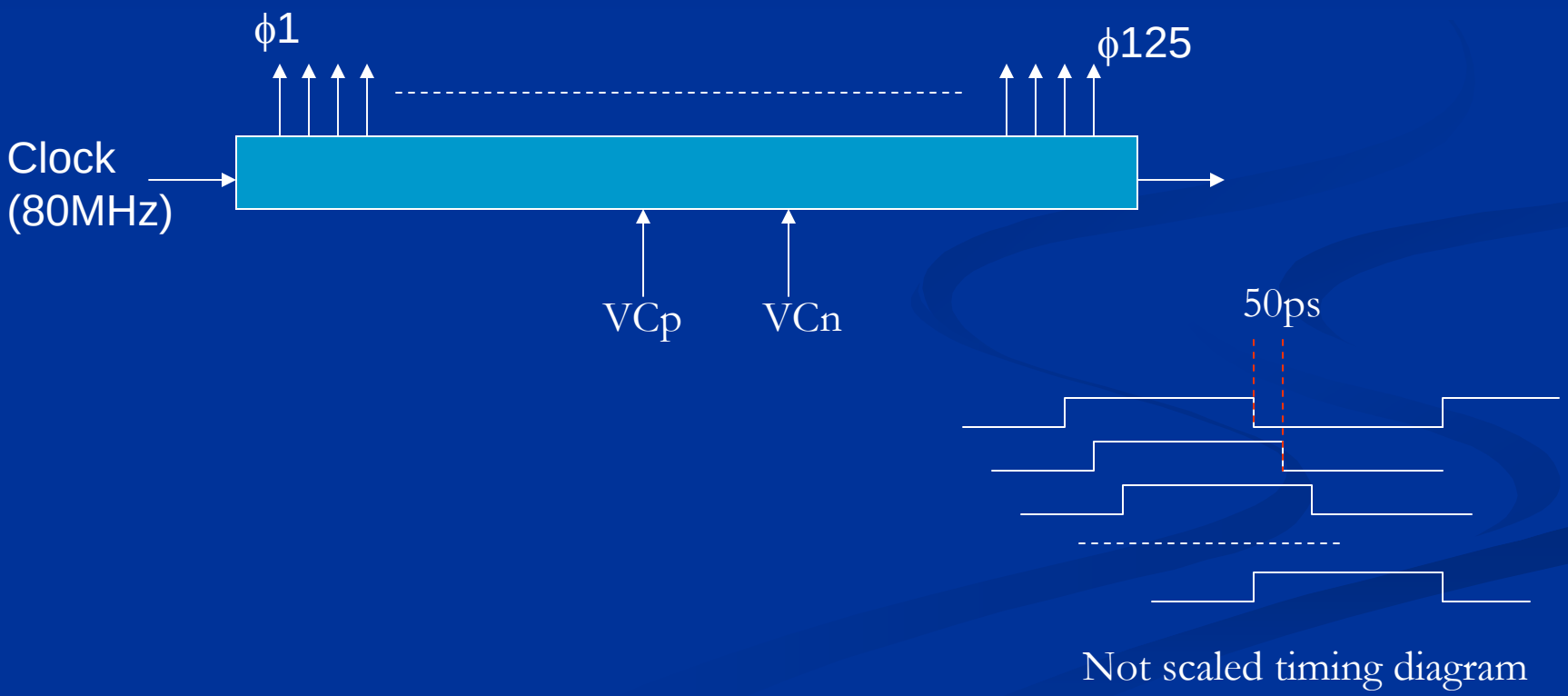
Principle of Timing Generator

Input Clock: 80MHz (T=12.5ns)

Output clock phases: 125/Cycle

Time delay per phase: 50ps

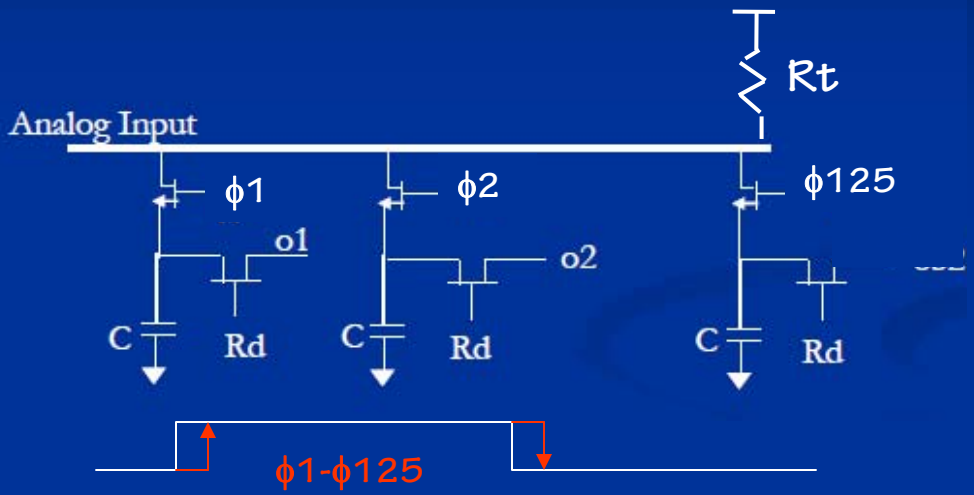
Voltage controlled time delay



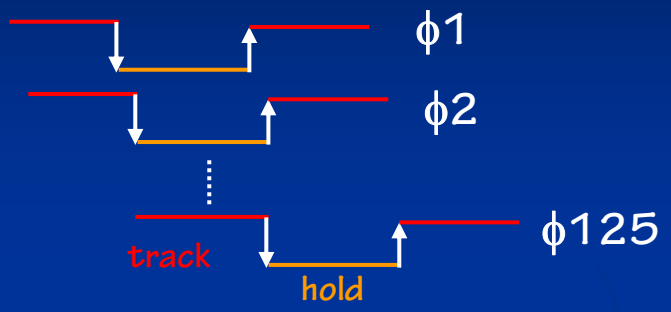
Not scaled timing diagram

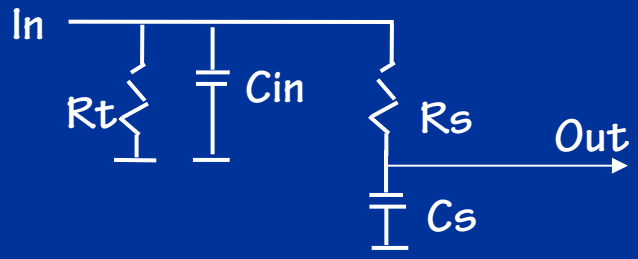
Track-and-Hold Timing & Sampling Bandwidth

Analog input pulse: Tr=Tf=Tw=100ps

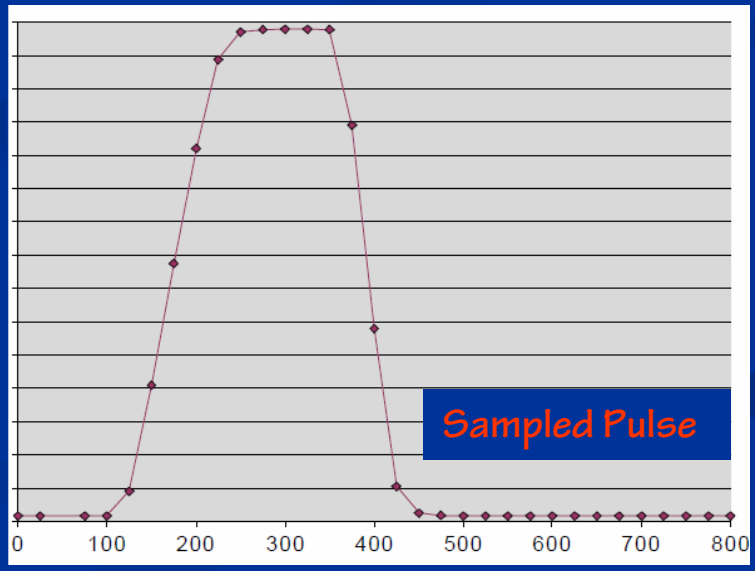


Switches of half a switch-chain are sequentially on for tracking, the rest of switches are sequentially off for holding.

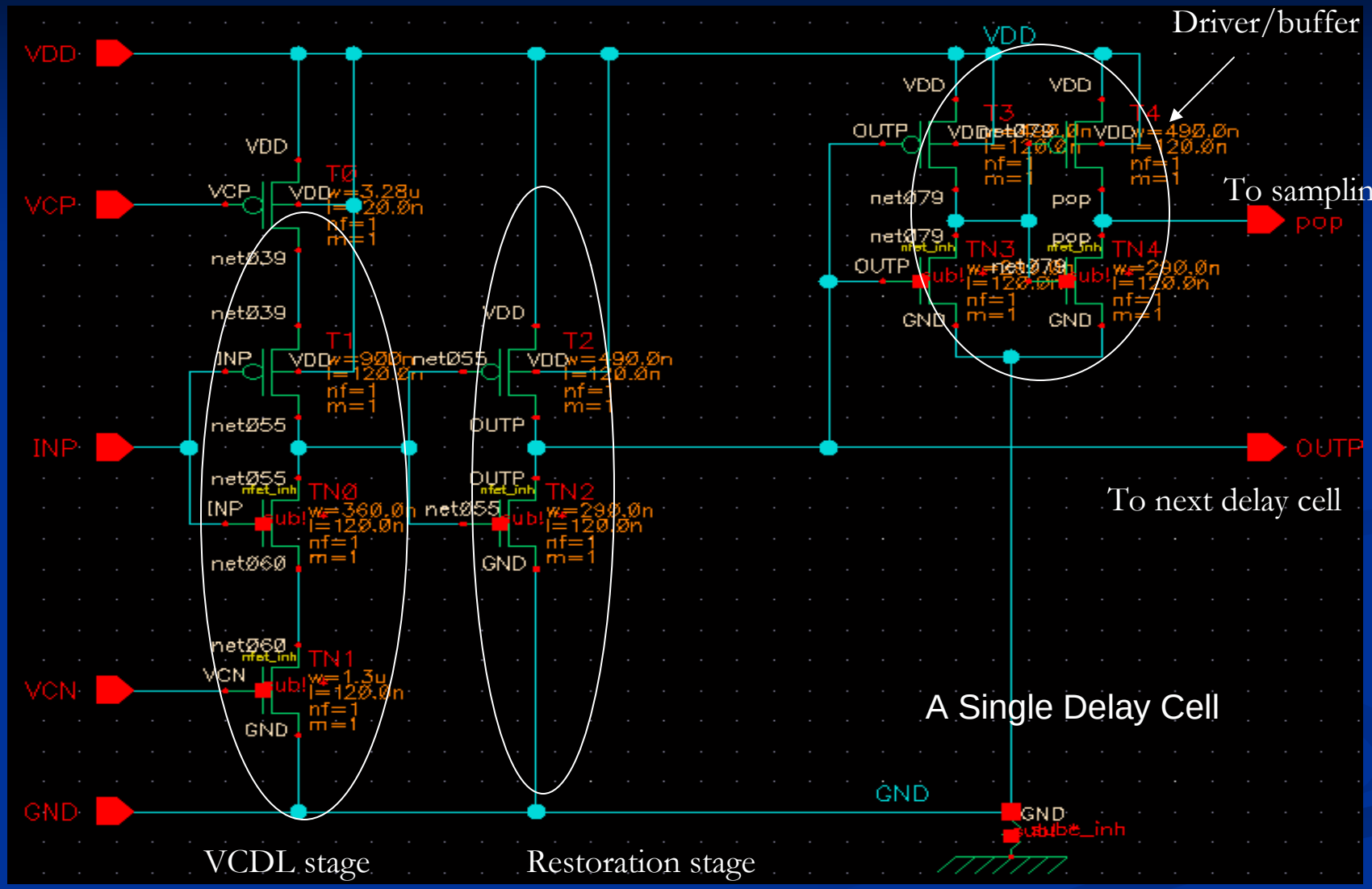




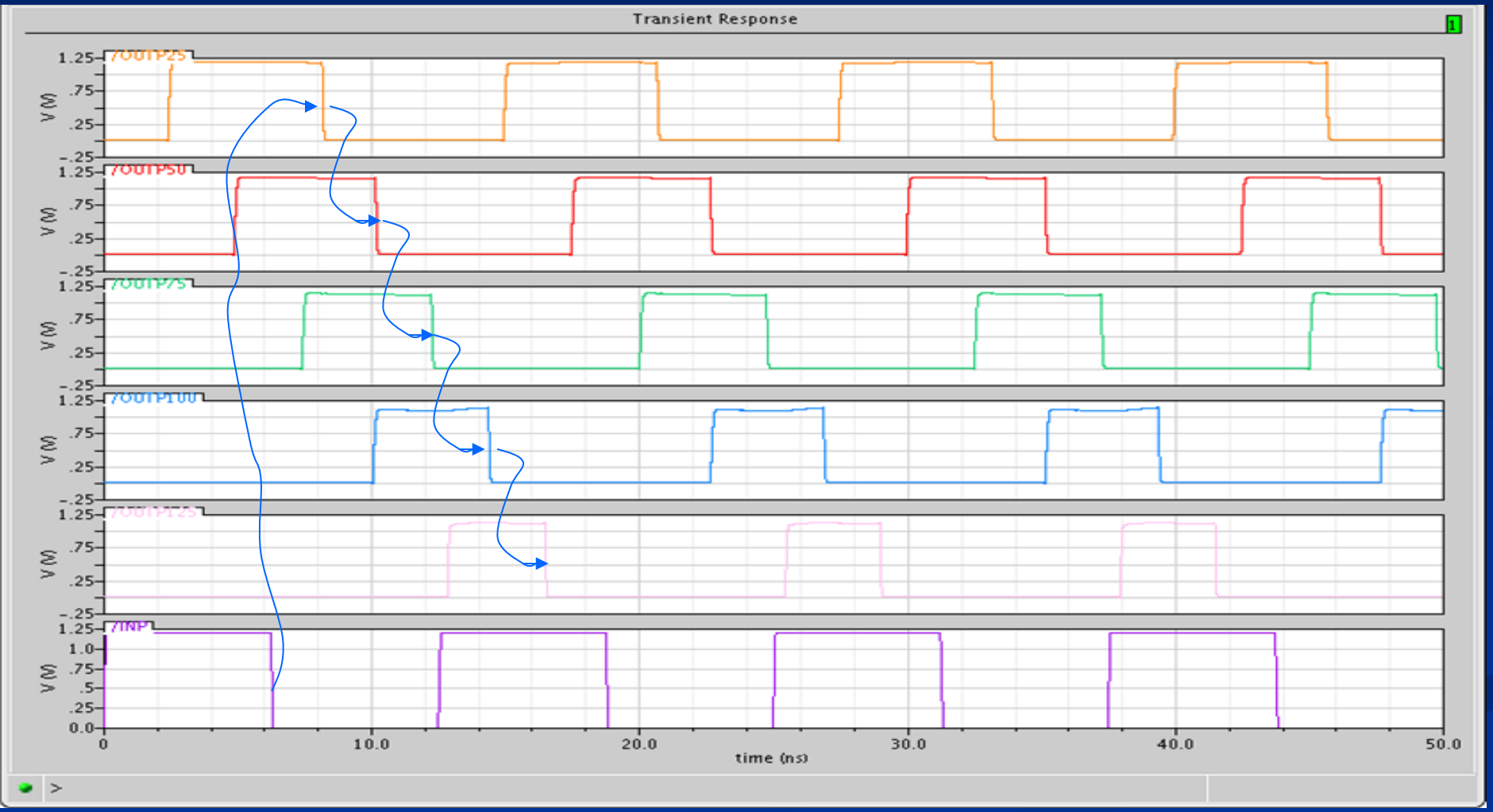
Analog Bandwidth is determined by a simplified 2-pole system



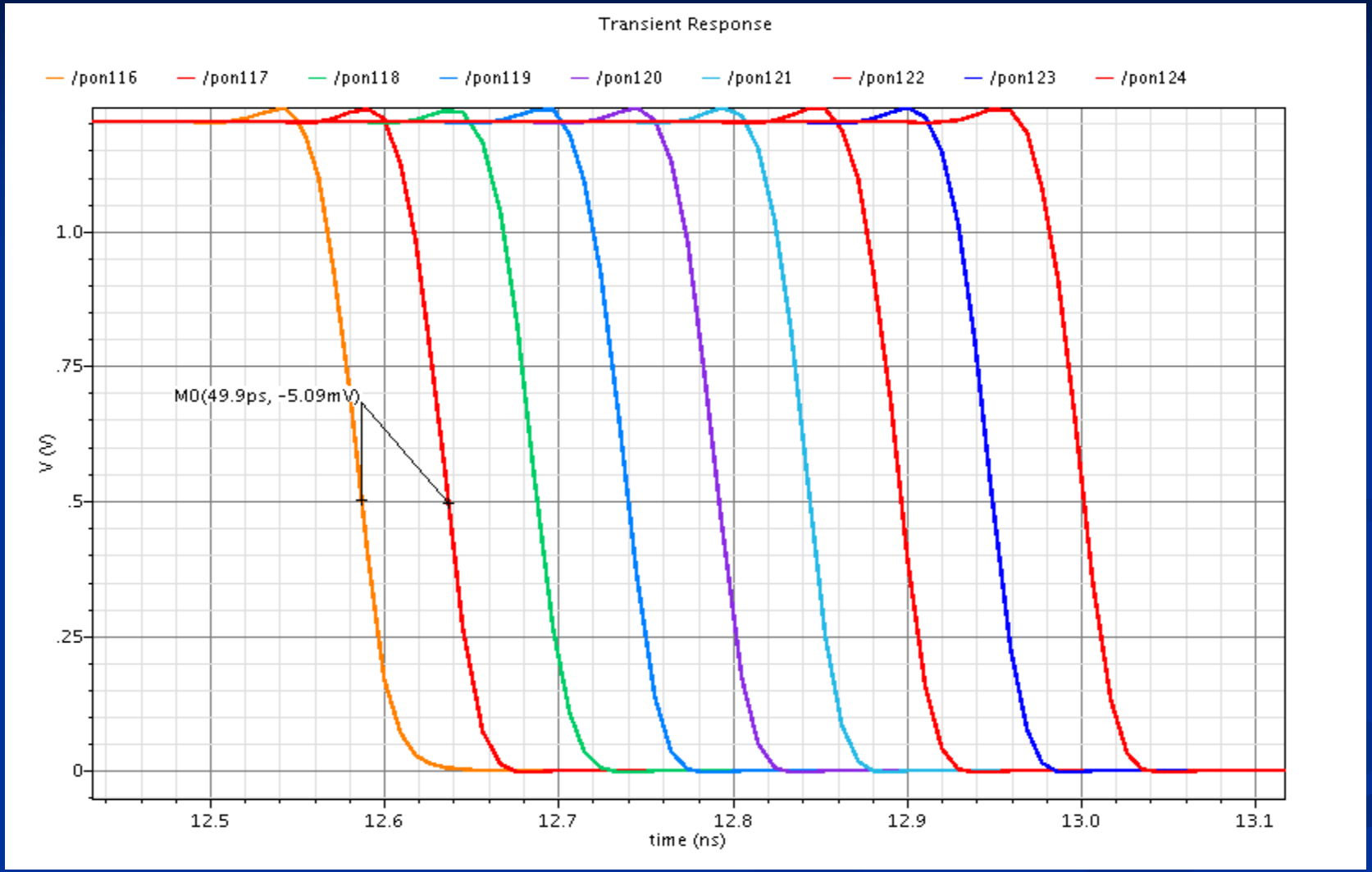
Current Starved Single-ended Voltage-Controlled Delay Cell



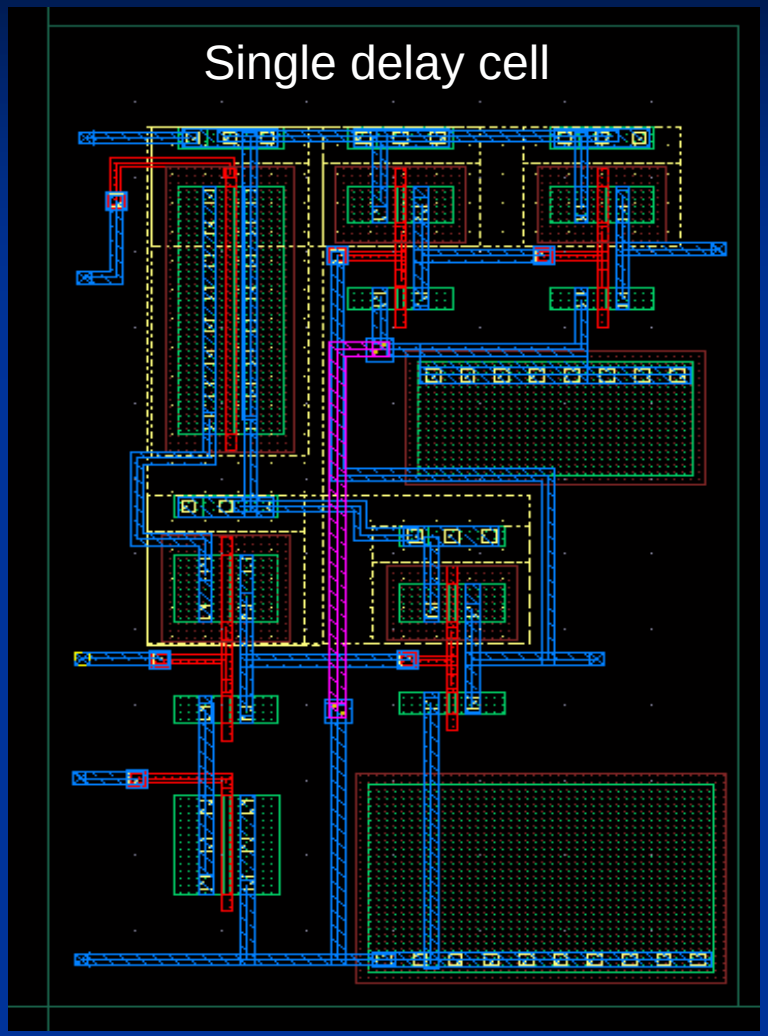
VCDL Simulation Results (125 Cells)



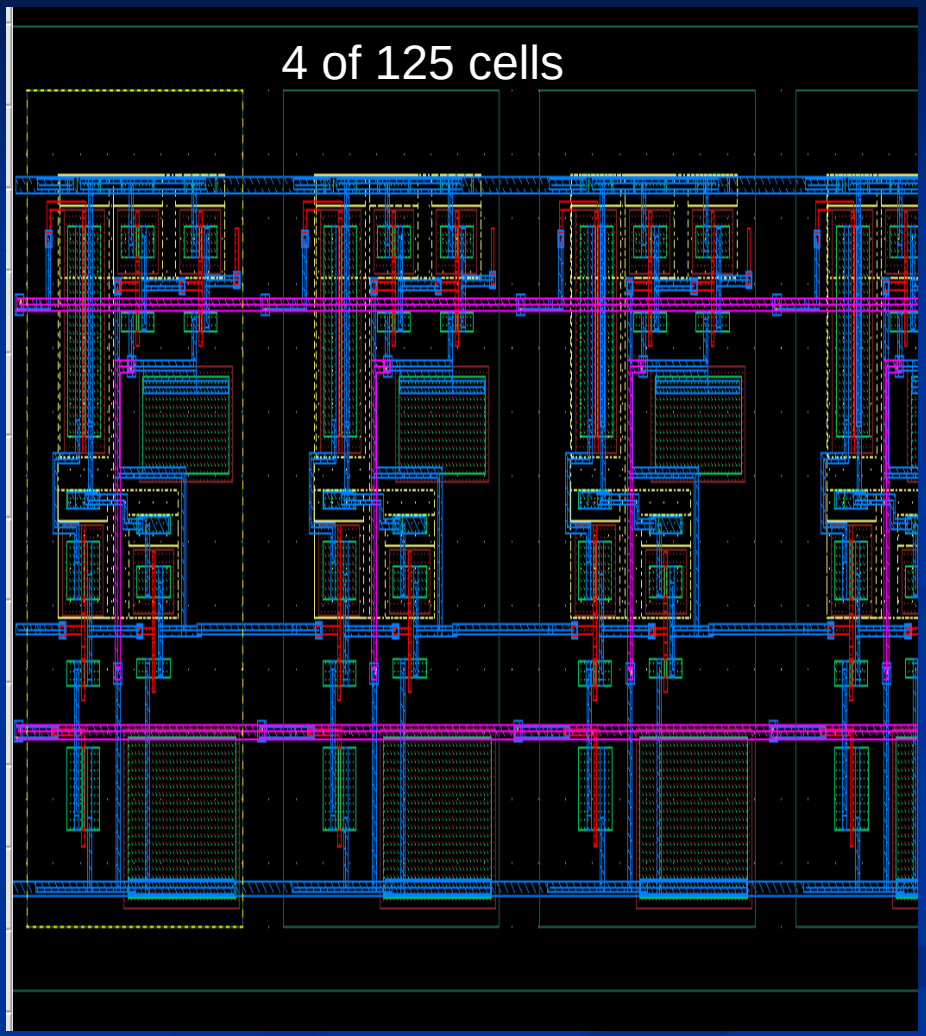
Phase Outputs from cell-116 to cell-124



Cell Layout

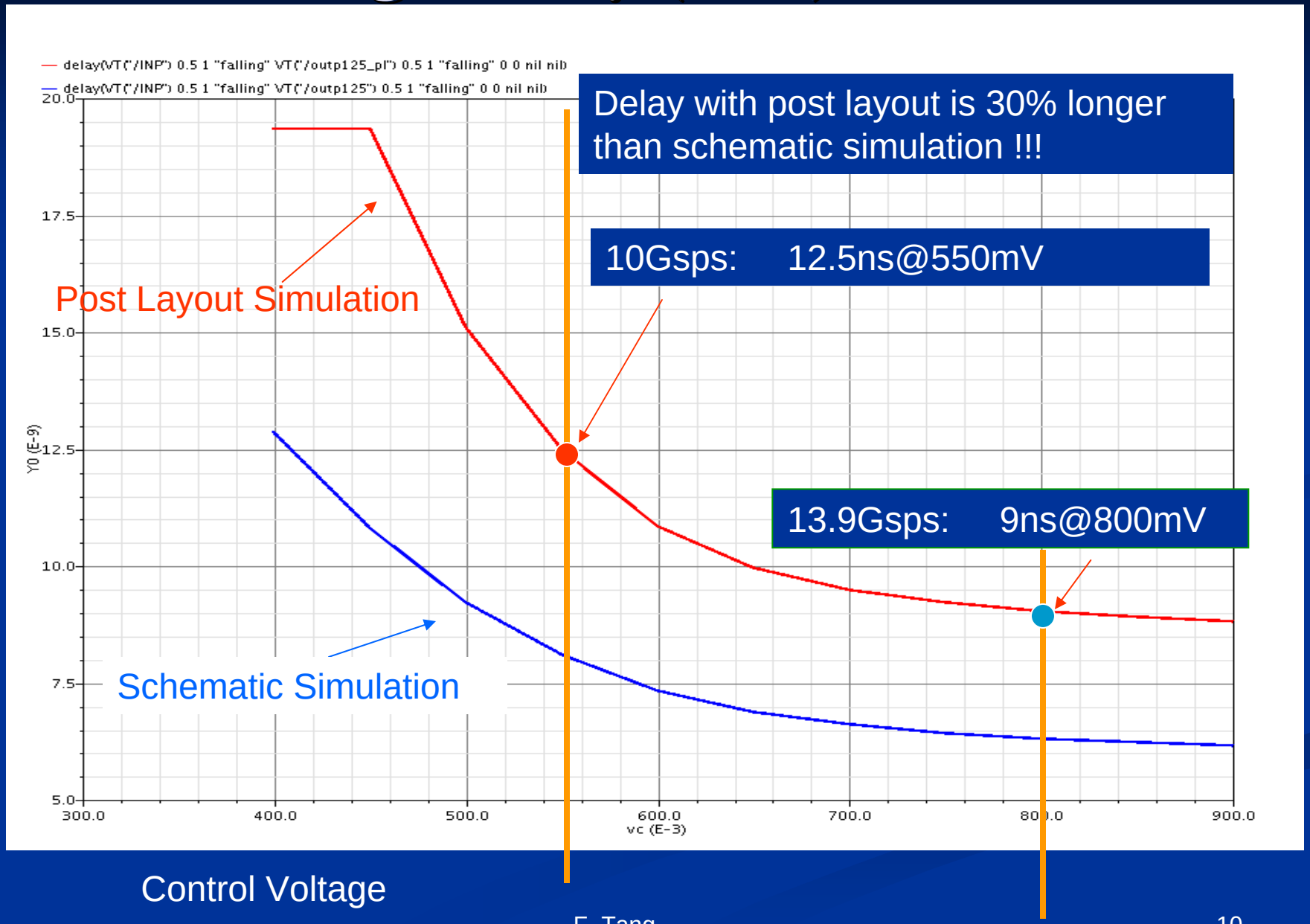


8 x 15 microns



1.2mm x 15 microns

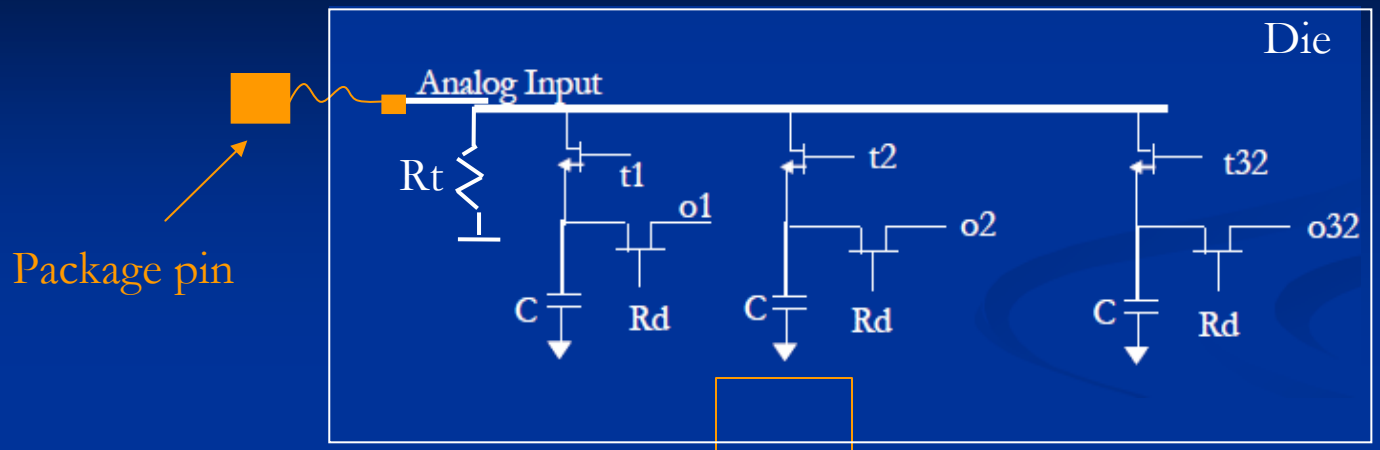
Voltage-Delay (V-D) Chart



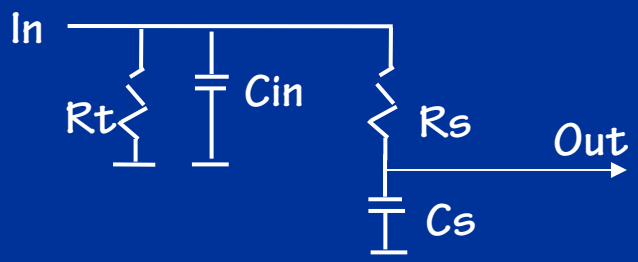
Discussion of Sampling Window

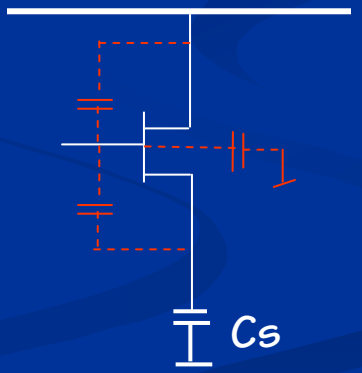
- Sampling window and input bandwidth.
- Minimum sampling window and sampling time constant
- Sampling window control logic

Sampling Window and Analog Input Bandwidth



Analog bandwidth can be modeled as a simplified 2-pole system

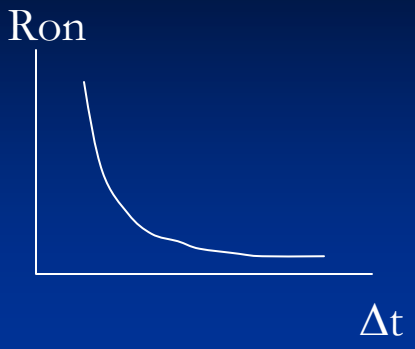


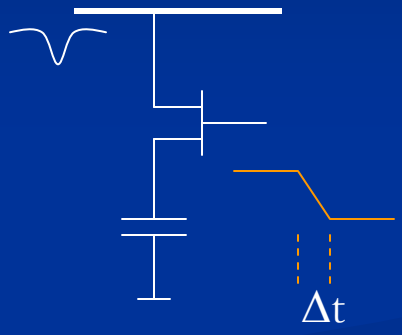


Cin=Cpkg + Cpad + Csw_on_all + Csw_off_all

Minimum Sampling Window and Sampling Time Constant

- Sampling time constant (RonCs)
- Switch on-resistance (Ron)
- Minimum sampling window:
  (Tw_min)= 2.2RonCs





If Ron = 4k, C = 40f. RonCs = 160ps

Tw_min = 2.2RonCs = 352ps → 7 sampling steps (50ps each)

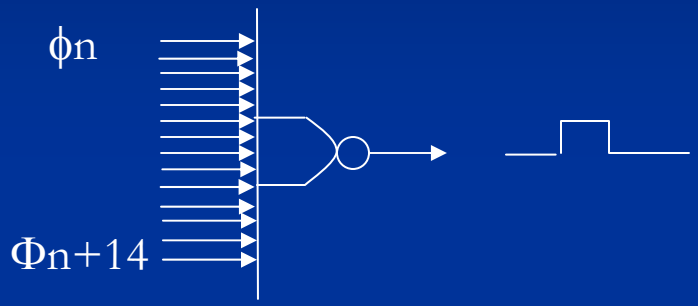
Assuming 2Tw_min used, then Tw should be set at lest 14 sampling steps (700ps).

Window Control Logic

- NAND gate:

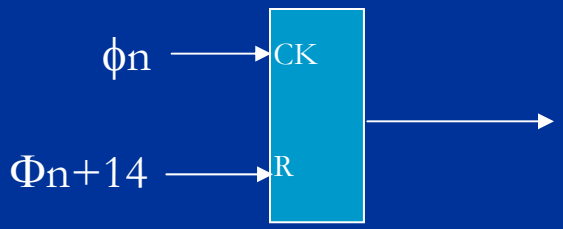
  A sample 14-input and gate can be used to set sampling window.

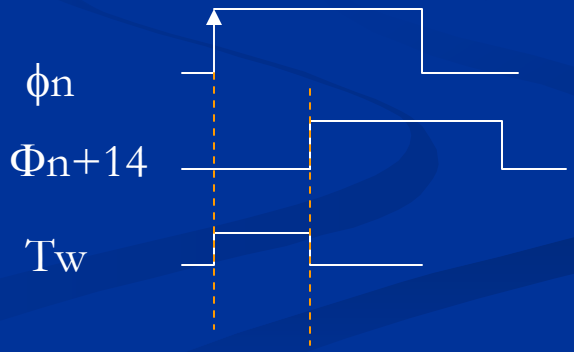
  ---disadvantage: Two many stages of circuitry to make AND14, each tap have to drive 14 loads



- (2) dff:

  -- disadvantage: too much layout area used.





Summary

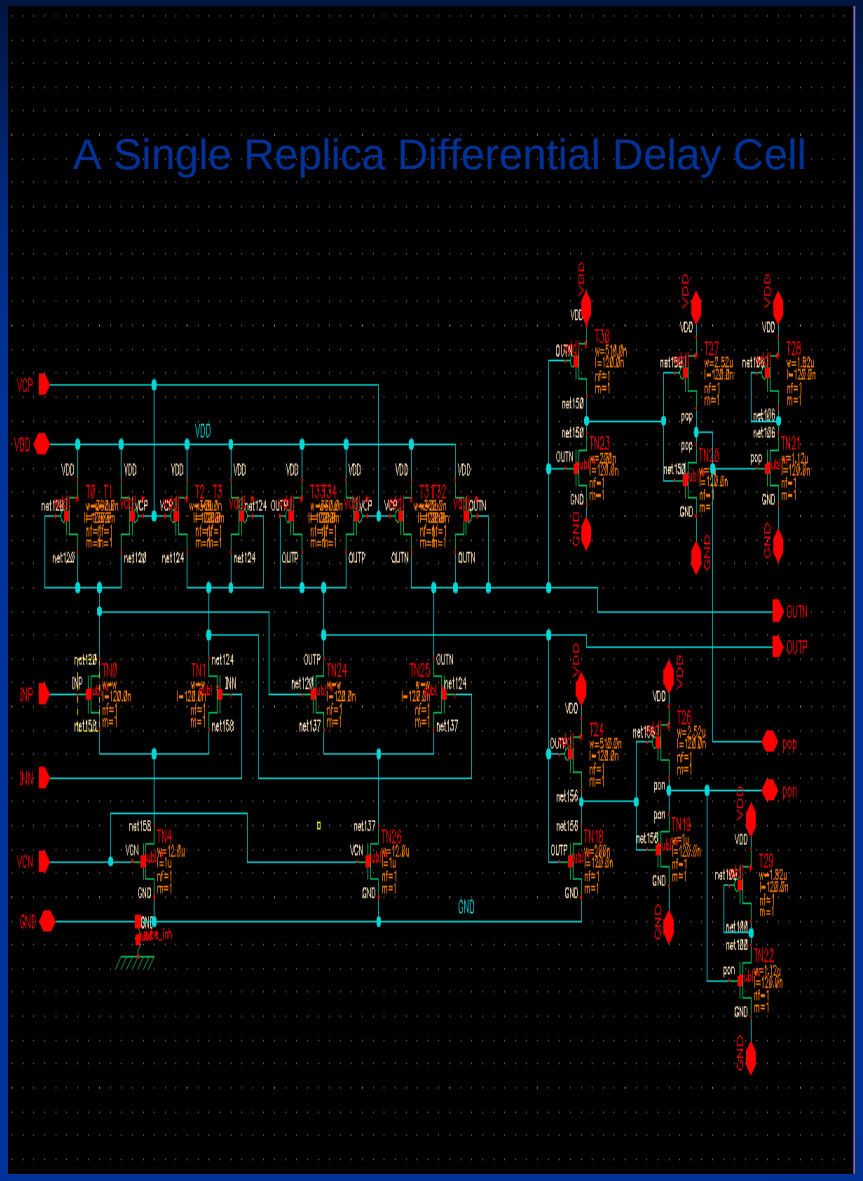
- Schematic and post layout simulations have been done.
- Post layout simulation showed a sampling rate of 10Gsps to 14Gsps can be achieved without interleaving.
- Same VCDL cell has been used for 2-GHz voltage controlled ring oscillator (see Emilien's talk).
- 125-cell schematic and layout blocks are available for top-level design.

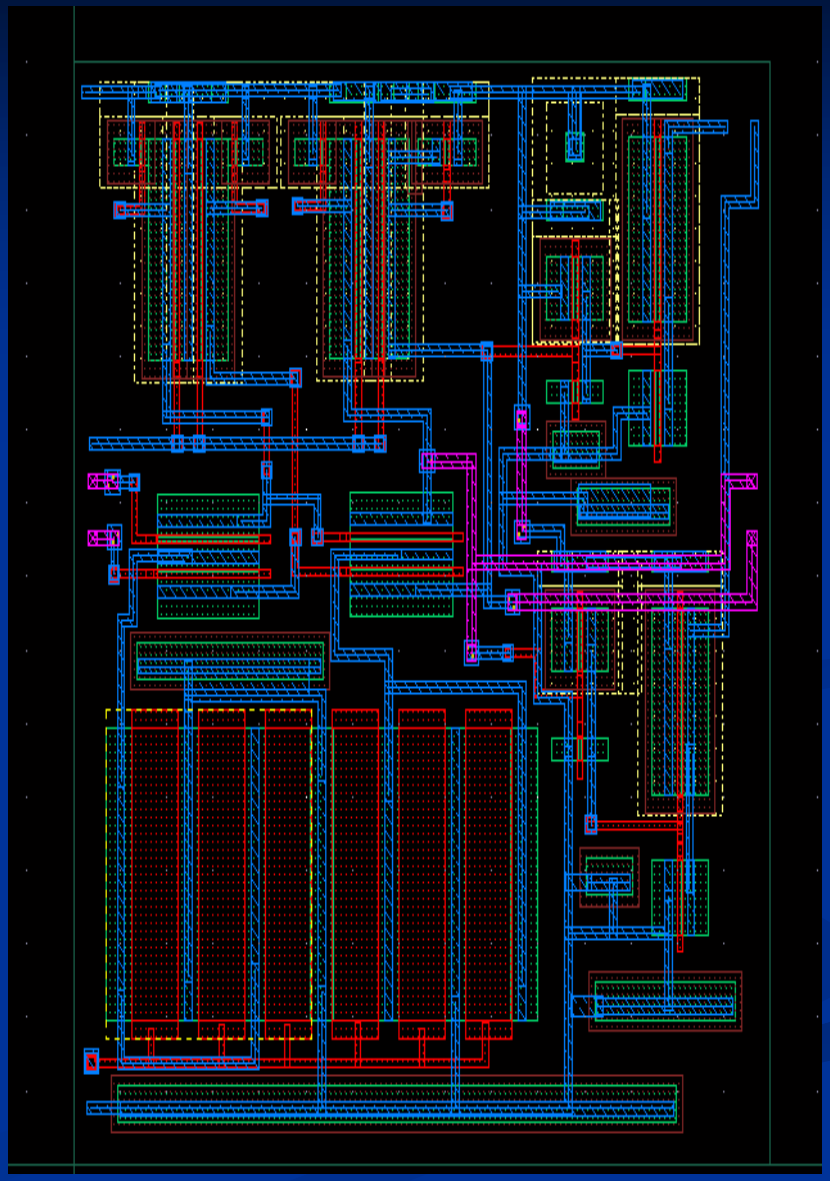
Thank you for your review

Backup Slides

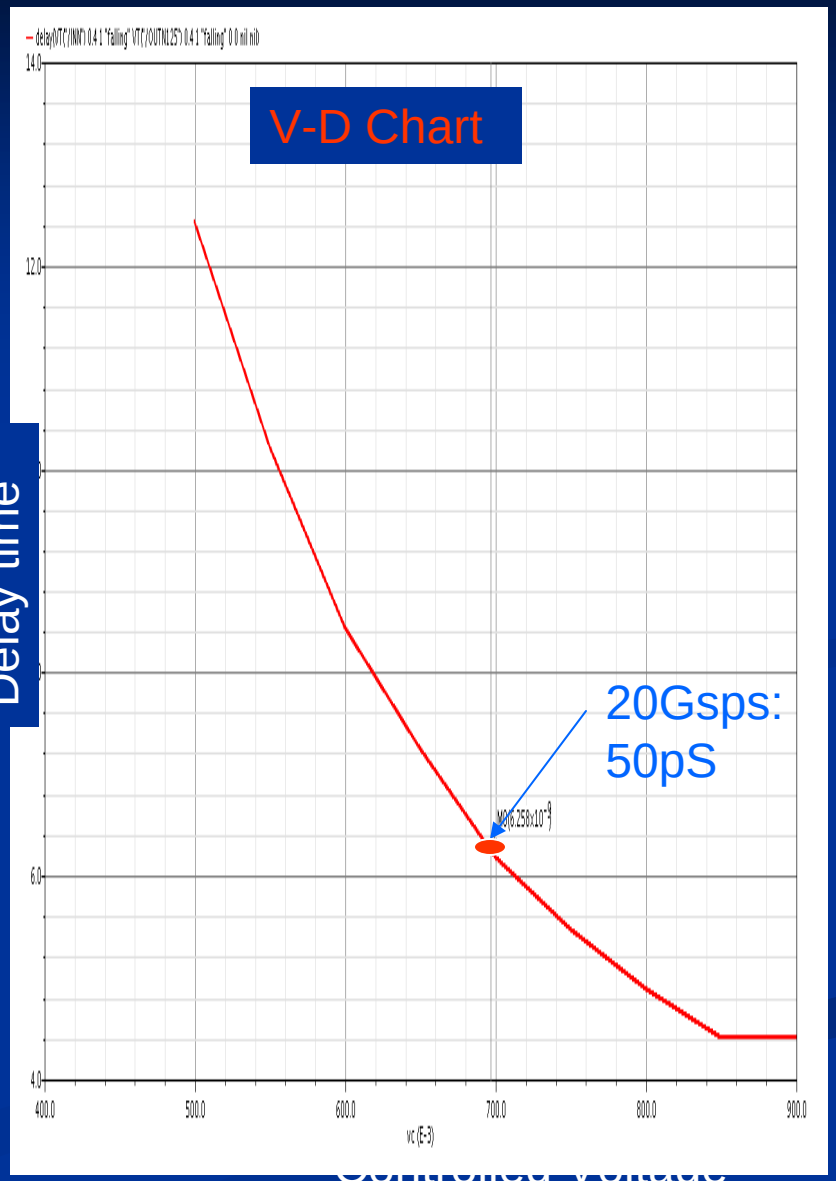
Why Not Differential VCDL?

Schematic and Layout of Replica Diff. Delay Cell



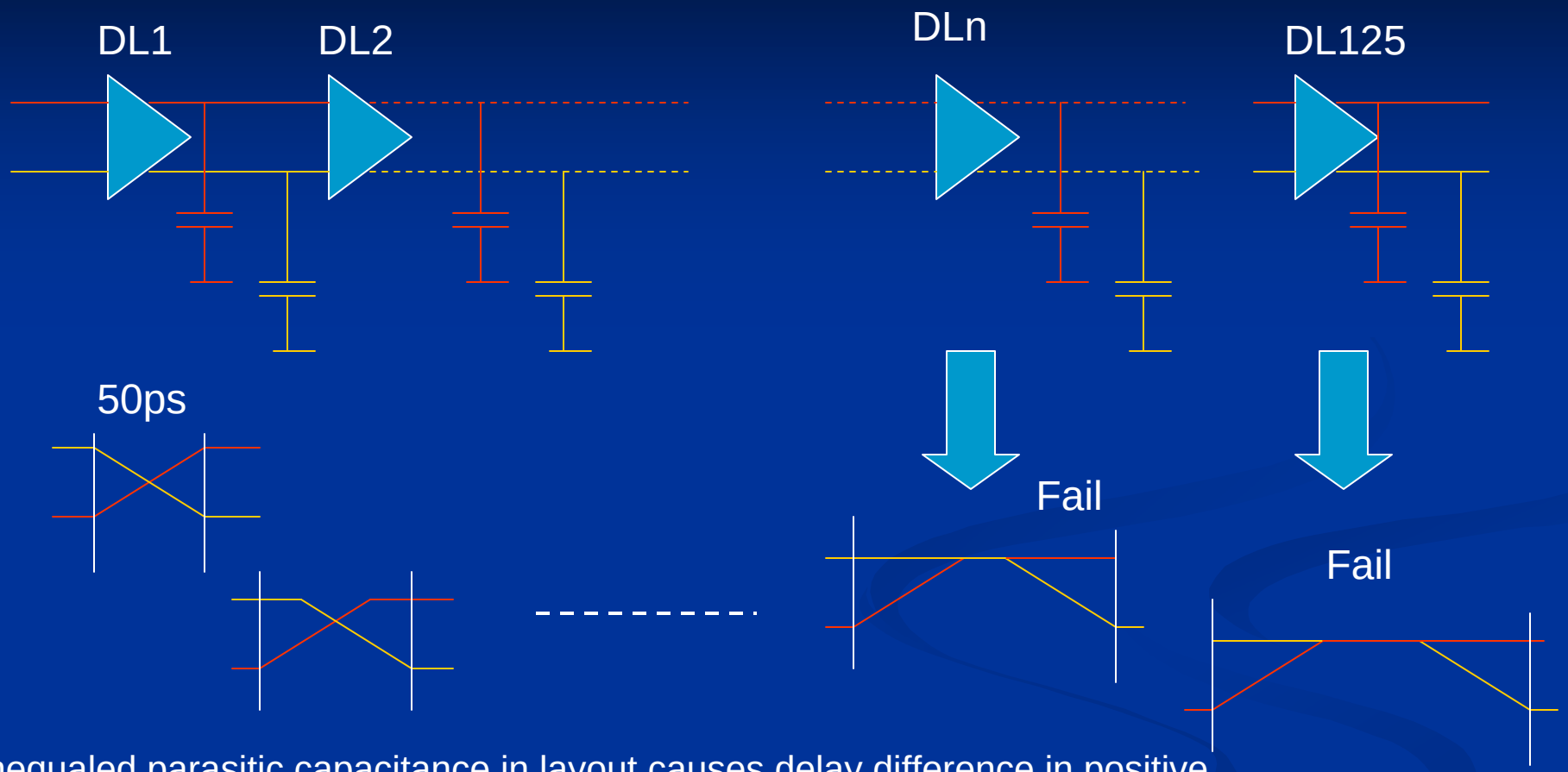


Schematic Simulation for 125 Cells



Controlled Voltage

Post Layout Simulation (Never Work!)

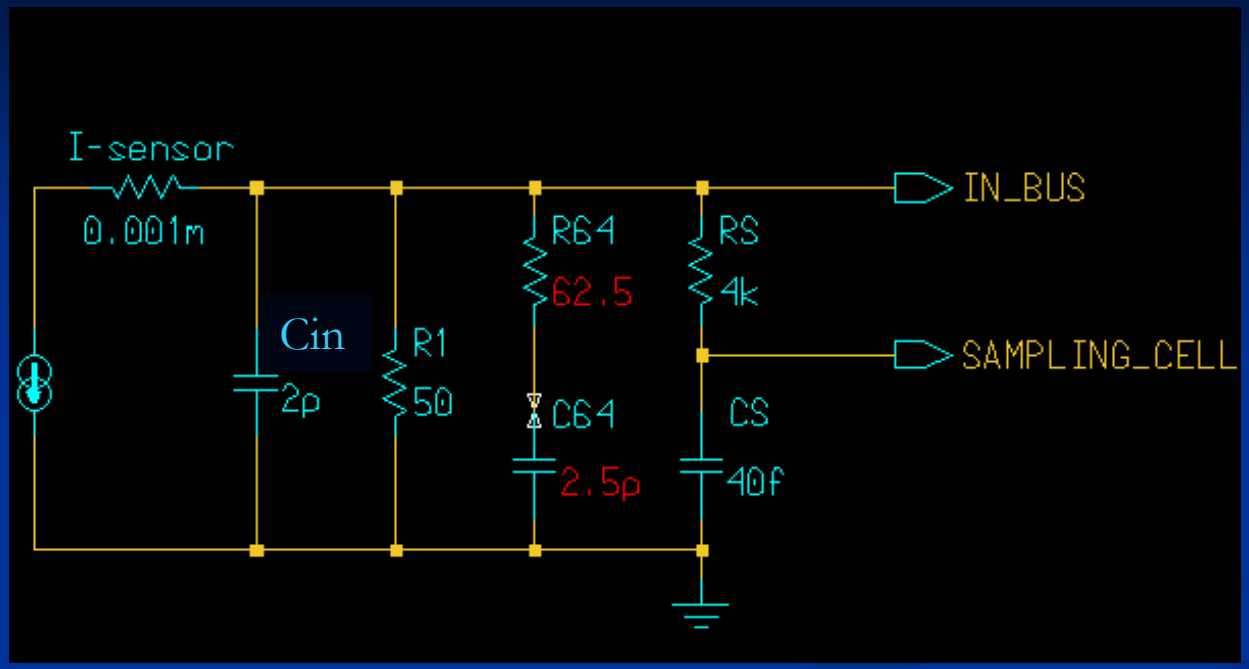


Unequaled parasitic capacitance in layout causes delay difference in positive and negative nodes of each cell. If accumulated delay difference is greater than 50ps in a chain of 125 cells, the delay chain went to malfunction. There is no way to tune the layout for such tight matching!

Backup Slide-2

Input Analog Bandwidth, Sampling Time Constant and Minimum Sampling Window

Modeling of Input Bus and Sampling Cells With Sampling Window of 3.25ns (64 cells)



64 cells in tracking, (3.2ns sampling window).

R64=4k/64 = 62 ohm

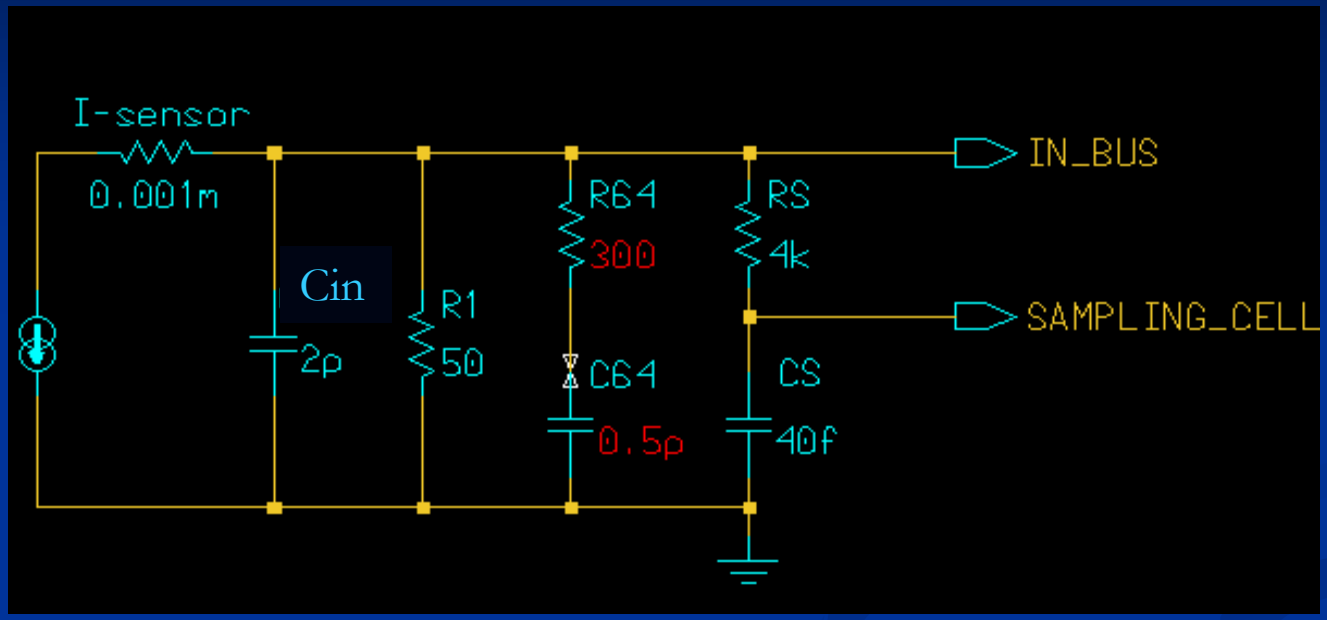
C64 = 4k * 40f = 2.5pF

Cin = 2pF

Cin=Cpkg + Cpad + Csw_on_all + Csw_off_all

Terminator = 50 ohms

Modeling of Input Bus and Sampling Cells With Sampling Window of 640ps (13 cells)



13 cells in tracking (640ps sampling window).

R64 = 4k/13 = 300 ohm

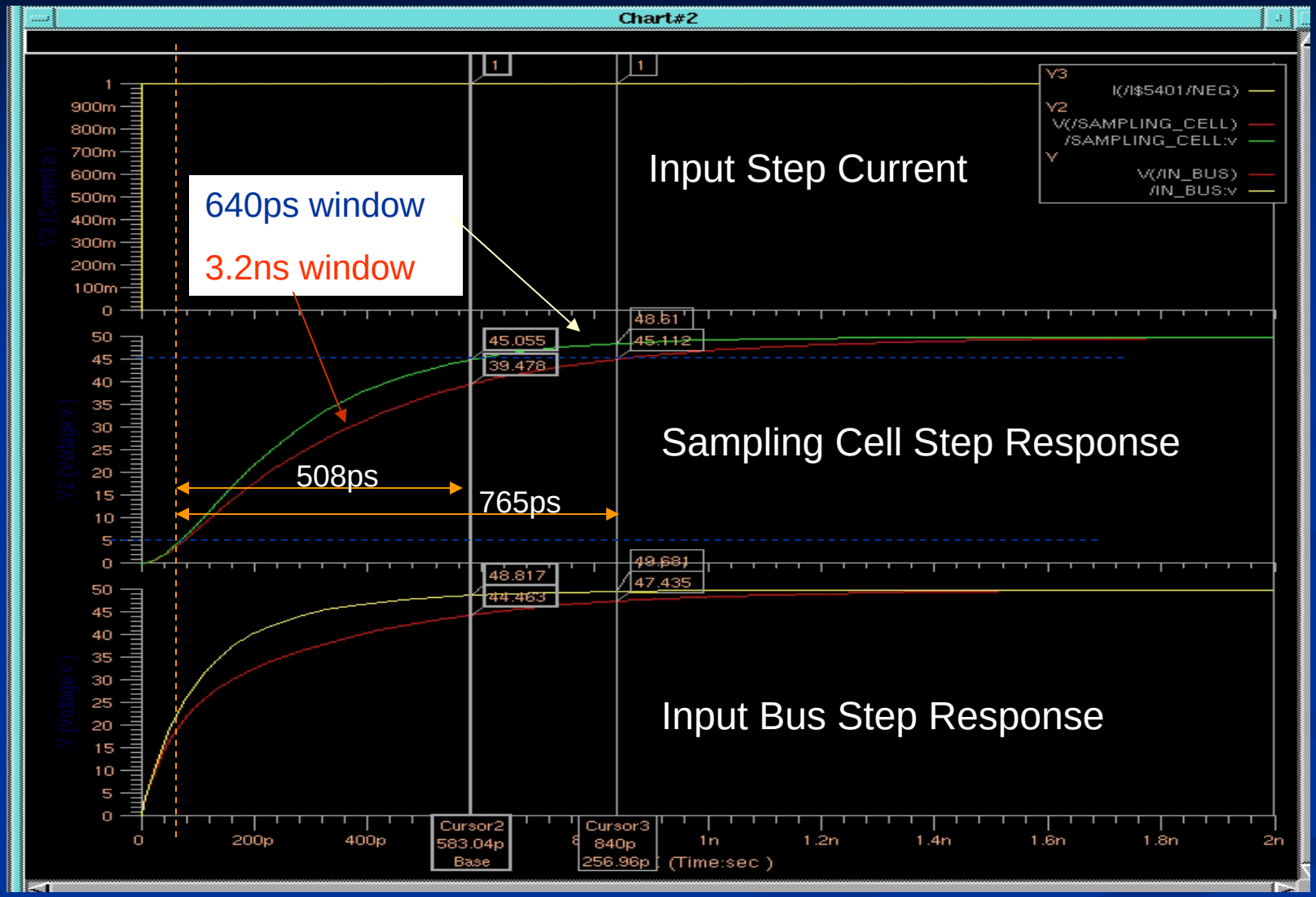
C64 = 13 * 40f = 0.5pF

Cin = 2pF

$Cin = Cpkg + Cpad + Csw_on_all + Csw_off_all$

Terminator = 50 ohms

Comparison of Simulation Results



From Step Response Simulations:

Sampling cell with 640ps sampling window, it has a rise time (10%-90%) of 508ps, equivalent to an analog bandwidth of 689MHz.

Sampling with 3.2ns sampling window, it has a rise time of 765ps, equivalent to an analog bandwidth of 457MHz.

We need simulate our circuits to evaluate our design for input analog bandwidth…