14-Bit, 500MHZ ADC Module for the KOTO Experiment at J-PARC

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Introduction

We present a new ADC/Data Processing Module, designed for Step 2 of the KOTO Experiment at J-Parc, Japan. The current KOTO Step 1 readout system occupies 18 VME crates and includes three distinctive blocks: the CsI calorimeter readout with 2,600 channels using custom 16-Channel, 14-Bit, 125MHz modules; the veto detector readout with 500 channels and the same type of ADC modules; and the beam hole veto detector readout with 100 channels and custom 4-Channel, 12-Bit, 500MHz ADC modules.

Our new 16-Channel, 14-Bit, 500MHz ADC/Data Processing Module has the same 6U VME64 form factor and power requirements as the above mentioned 14-Bit, 125MHz modules, and it is designed to replace all readout modules with great improvements in overall performance.

Architecture

The Block Diagram for the ADC module is presented in Figure 1.

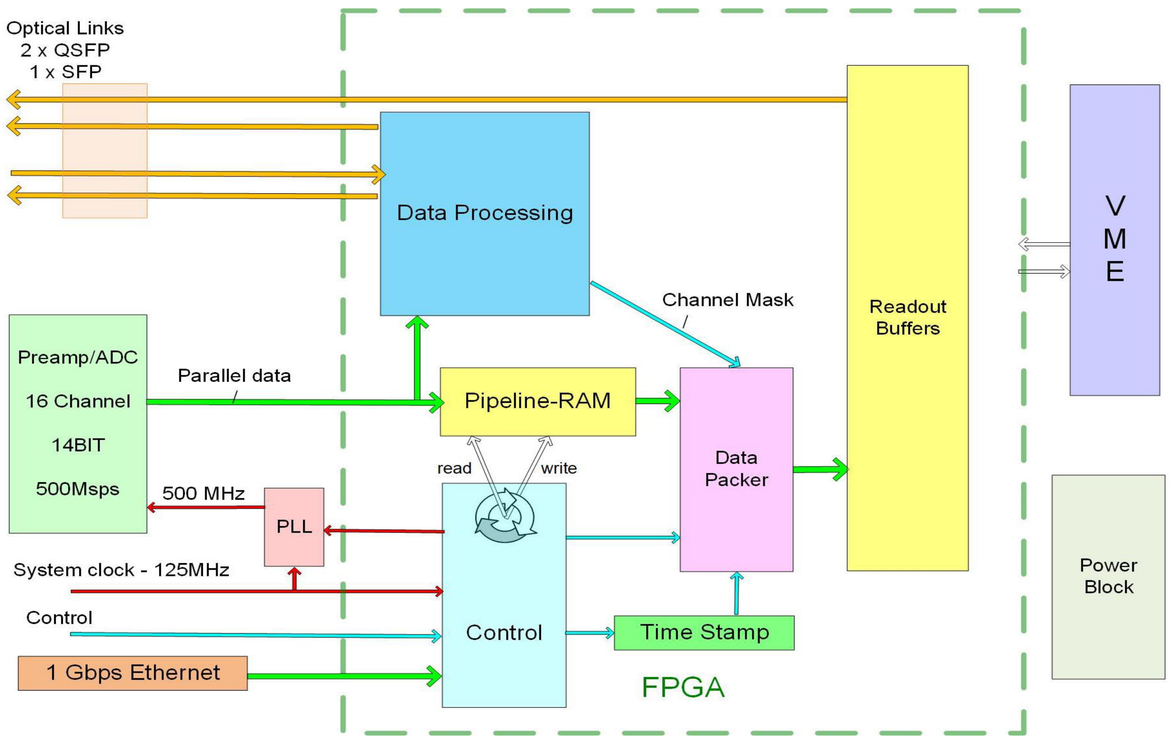

Figure1. Block Diagram of the 500MHz ADC Module.

We can identify four main blocks: the signal conditioning and conversion block with 8 pieces dual ADC chips, the data processing block with one FPGA, the power block and the interface block.

Using a local PLL, the module generates the 500MHz sampling clock in sync with the 125MHz system clock, and this allows for simultaneous sampling of all 3,100 DAQ channels.
For other applications, the module can run independently, on a locally generated clock.

In KOTO, analog signals are passed in CAT6 Cables, with only two pairs being used, and the ADC modules have two differential inputs on each RJ45 connector, while 4 pins are grounded. This configuration was proven to perform best with respect to crosstalk.

Two analog signals are buffered and applied to one AD9684BBPZ-500. The FPGA receives the samples in parallel interleaved mode at 1,000Mbps from each ADC chip.

All 16 channels are serviced by one single 5AGXFB7H4F35C4N. The 500 MHz digitized samples are first deserialized and reduced in frequency by a factor of four. All subsequent data processing steps take place at the 125MHz system clock frequency.

Figure 2 presents the schematic of one analog channel, configured for the differential with offset signal used in KOTO. Input bandwidth is 125MHz at -3dB.

There are two QSFP transceivers with up to 5Gbps per link, for a total of 40Gbps. Depending on the application and data rate requirements, all 16 channels can be read out from any of the QSFPs, or from both.

The VME64 backplane provides an alternative path for configuration and low-rate data readout, but it is mostly used for initial testing and debugging.

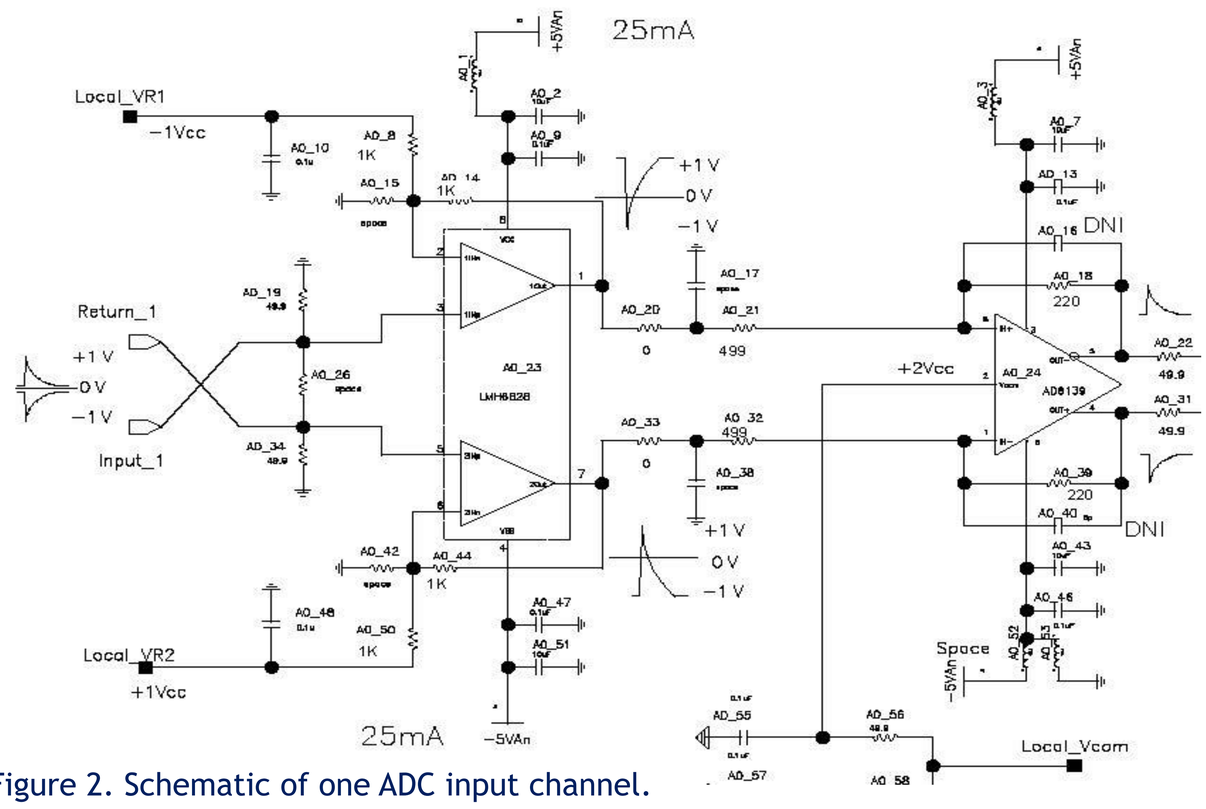

Figure 2. Schematic of one ADC input channel.

Board configuration can be done either via a front panel SFP link or Ethernet port, while an auxiliary RJ45 connector with 4 LVDS lines can be used for system clock synchronization and triggering.

Conclusions

Figure 3 presents one of the ADC modules. Preliminary test results show an input noise of about 2.8 LSB for a sampling rate of 500MHz, and with a one-pole input filter at about 125MHz.
This small and powerful ADC module was designed to be used in the KOTO DAQ System.
With minor firmware changes, and/or passive component modifications, this module can be easily integrated in many other applications.

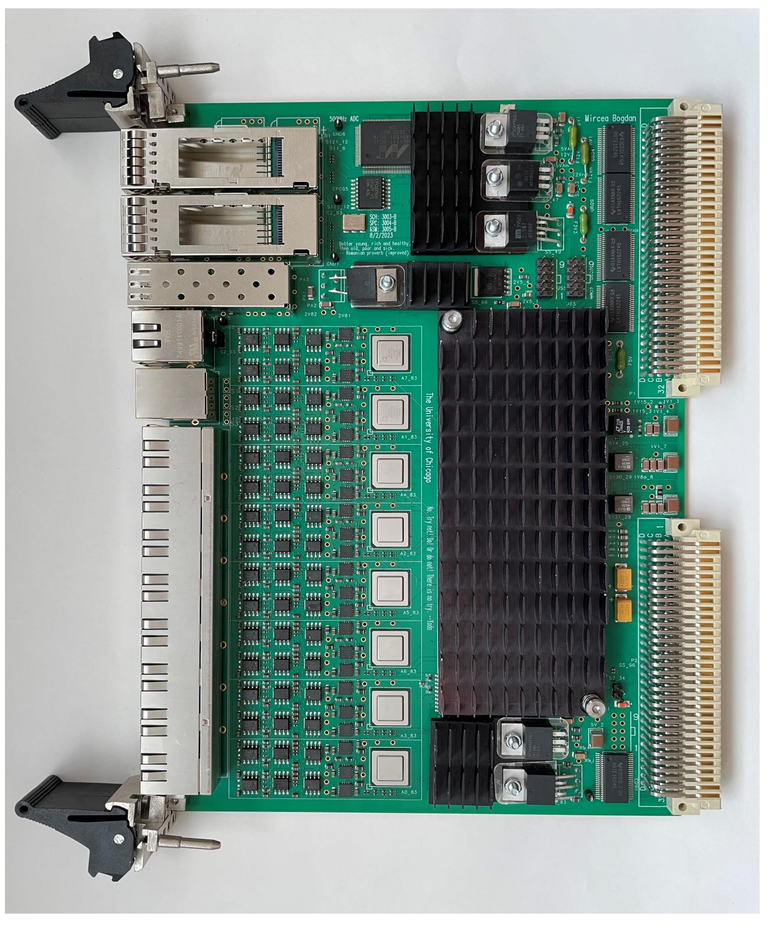

Figure 3. Prototype 16-Channel. 14-Bit 500MSPS ADC