We present a new ADC/Data Processing Module, designed for Step 2 of the KOTO Experiment at J-PARC. The current KOTO Step 1 readout system occupies 18 VME crates and includes three distinctive blocks: the CsI calorimeter readout with 2,600 channels using custom 16-Channel, 14-Bit, 125MHz modules; the veto detector readout with 500 channels and the same type of ADC modules; and the beam hole veto detector readout with 100 channels and custom 4-Channel, 12-Bit, 500MHz ADC modules.

Our new 16-Channel, 14-Bit, 500MHz ADC/Data Processing Module has the same 6U VME64 form factor and power requirements as the above mentioned 14-Bit, 125MHz modules, and it is designed to replace all readout modules with great improvements in overall performance.

The Block Diagram for the ADC module is presented in Figure 1.

We can identify four main blocks: the signal conditioning and conversion block with 8 pieces dual ADC chips, the data processing block with one FPGA, the power block and the interface block.

Using a local PLL, the module generates the 500MHz sampling clock in sync with the 125MHz system clock, and this allows for simultaneous sampling of all 3,100 DAQ channels. For other applications, the module can run independently, on a locally generated clock.

In KOTO, analog signals are passed in CAT6 Cables, with only two pairs being used, and the ADC modules have two differential inputs on each RJ45 connector, while 4 pins are grounded. This configuration was proven to perform best with respect to crosstalk.

Two analog signals are buffered and applied to one AD9684BBPZ-500. The FPGA receives the samples in parallel interleaved mode at 1,000MSPS from each ADC chip.

All 16 channels are serviced by one single 5AGXF74H4F35C4N. The 500 MHz digitized samples are first deserialized and reduced in frequency by a factor of four. All subsequent data processing steps take place at the 125MHz system clock frequency.