16-Channel, 14-Bit, 500 MHz ADC Module

The University of Chicago

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16-Channel, 14-Bit, 500MHz ADC Board

Populated two Modules, received - 1/20/23
- One module with just two ADC chips
- One module with no ADC chips

Started testing

http://edg.uchicago.edu/~bogdan/14BIT_500MHz_ADC_Board/schematics.html
16-Channel, 14-Bit, 500MHz ADC Board

Same Front End Circuit as Old 500MHz ADC Module

Two ADC Channels per Chip

AD9684BBPZ-500
16-Channel, 14-Bit, 500MHz ADC Board

Schematic Problem
Connection Fix:
- Remove output inductors for these 3 LDOs (8 times/board)
- Change AVDD_1.8V to 1.25V = change one resistor only
- Bypass 2 LDOs with wires (8 times)
- Bring 2.5V from other side of the board with wires (8 times)
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ADC chip AD9684 - Data Sheet Problem 1:

Data Sheet: Chip starts in “one converter mode”, and internal register 0x568 needs to be changed from 0x00 to 0x01, to have two converters working.

Designed VME controlled SPI to change the ADC chip internal register. Default value for internal register 0x568 is actually 0x01 and Data Sheets is Wrong! ADC chips starts in two converter mode without register changes. Data Sheet error was confirmed by AD technical support team.

<table>
<thead>
<tr>
<th>Reg. Addr. (Hex)</th>
<th>Register Name</th>
<th>Bit 7 (MSB)</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0 (LSB)</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x568</td>
<td>LVDS output mode</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Output data mode</td>
<td>0x00</td>
<td>000 = parallel mode (one converter) 001 = parallel interleaved mode (two converters) 010 = parallel channel multiplexed (even/odd) mode (one converter) 011 = parallel channel multiplexed (even/odd) mode (two converters) 100 = byte mode (one converter) 101 = byte mode (two converters) 110 = byte mode (four converters) Others = reserved</td>
<td></td>
</tr>
</tbody>
</table>

| 0x569            | Digital clock output adjust | 0           | 0     | 0     | 0     | 0     | 0     | DCO phase adjustment | 0x00    | 0x0: 0° 0x1: 90° 0x2: 180° 0x3: 270° |

| 0x01 |
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ADC chip AD9684 - Data Sheet Problem 2:

Data Sheet: Chip sends a “Ramp output” when configured in test mode “1111”

Used VME controlled SPI to set the ADC chip in corresponding test mode.

Data Sheets is Wrong!
In that test mode, ADC chip sends out a counter, but every word is repeated 4 times!
This suggests a logic or a timing error in the FPGA design.

-> Time spent chasing inexistent hardware issue...

Data Sheet error was confirmed by AD technical support team.
16-Channel, 14-Bit, 500MHz ADC Board
ADC chip AD9684 - Data Sheet Problem 2:

VME recorded data with ADC chip in test mode – ramp output

VME recorded data with sine wave at the input of the board
Preliminary Tests:

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5 MHz Differential Input Signal

VME recorded data

Recording with signals to both ADCs inside one chip
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To do:

- Install 8 ADC chips (16 channels) on the 2\textsuperscript{nd} module

- Continue testing:
  - Total Power, Noise, X-talk etc.