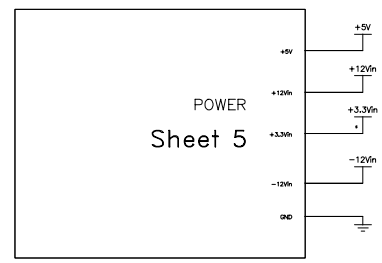
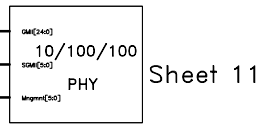
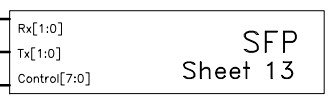
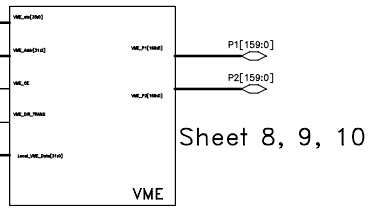
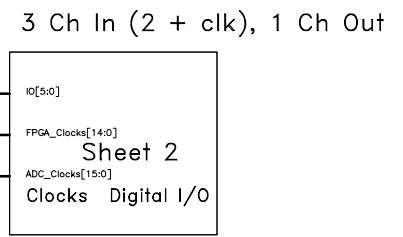


FPGA
Sheet 6, 7



SCH# 3003
SPC# 3004
ASM# 3005

Engineer: M. Bogdan	The University of Chicago Top Level 500MHz 16Ch ADC Module
Drawn by: M. Bogdan	
DATE: 2/10/2022	
REV. A	DRW. 3003 Sheet 1