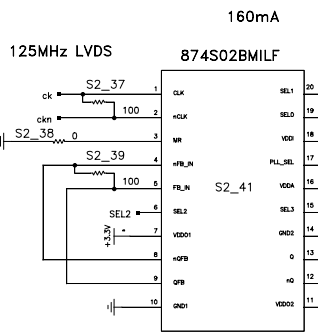
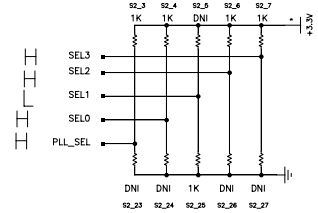
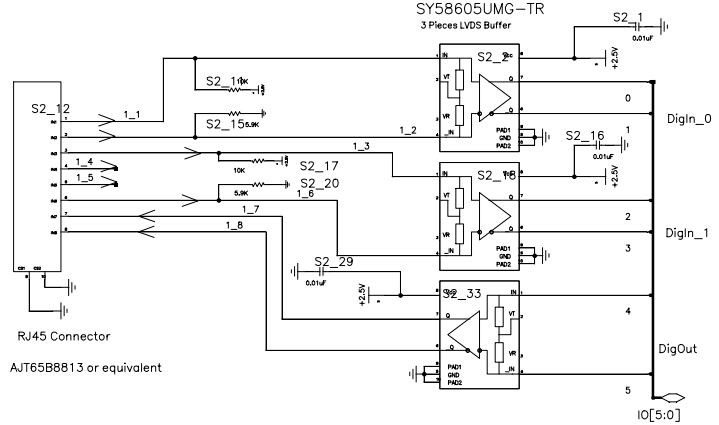


3 x 50mA = 0.15A  
 SY58605UMG-TR  
 3 Pieces LVDS Buffer

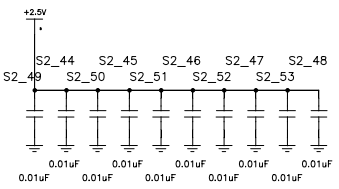
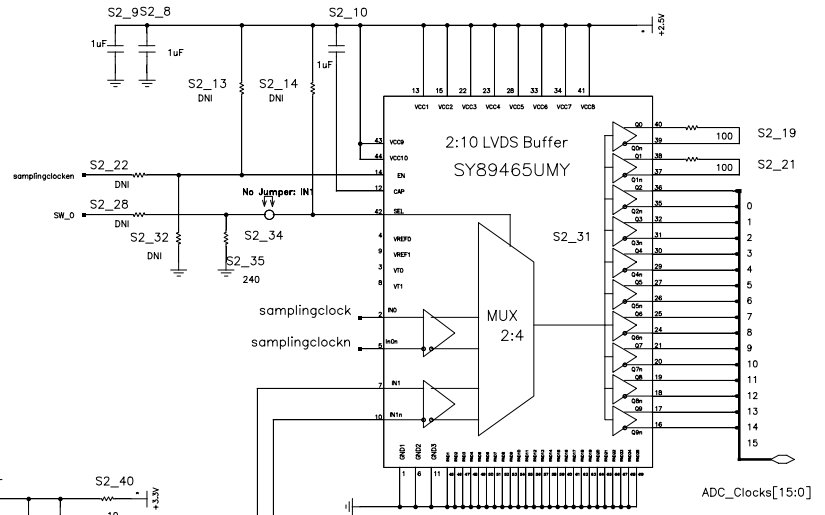


160mA

125MHz LVDS

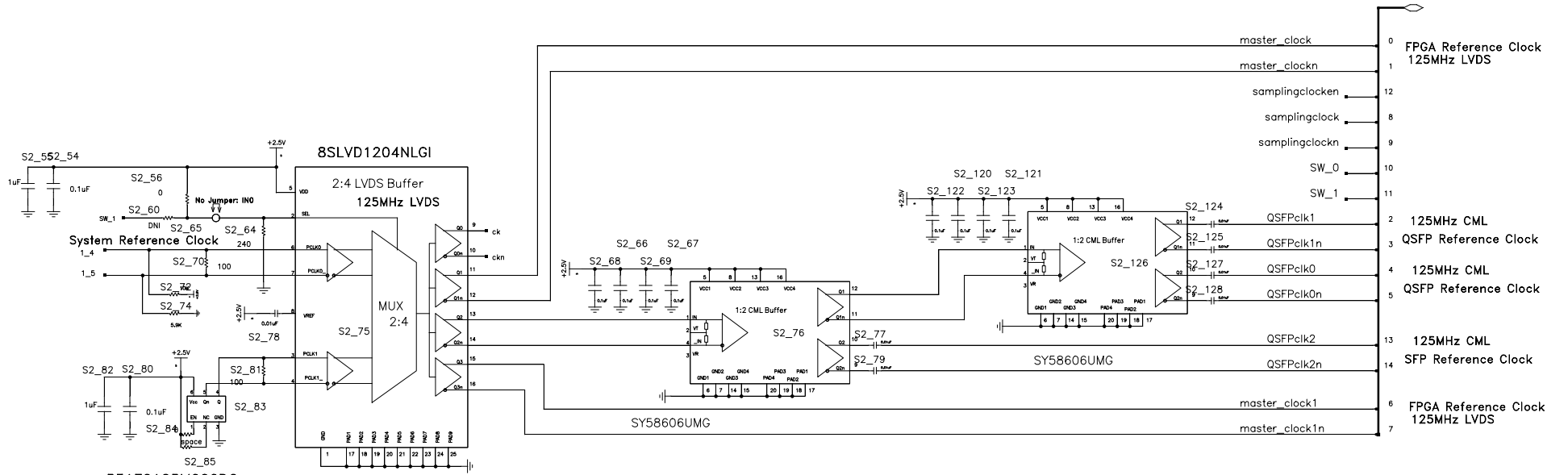
500MHz LVDS

0.3A



531FC125M000DG  
 Internal Reference Clock  
 125MHz LVDS

FPGA\_Clocks[14:0]



Engineer:	M. Bogdan	The University of Chicago Digital Input and Clocks 500MHz 16Ch ADC Module	
Drawn by:	M. Bogdan		
DATE:	2/7/2022		
REV. A	DRW.	3003	Sheet 2