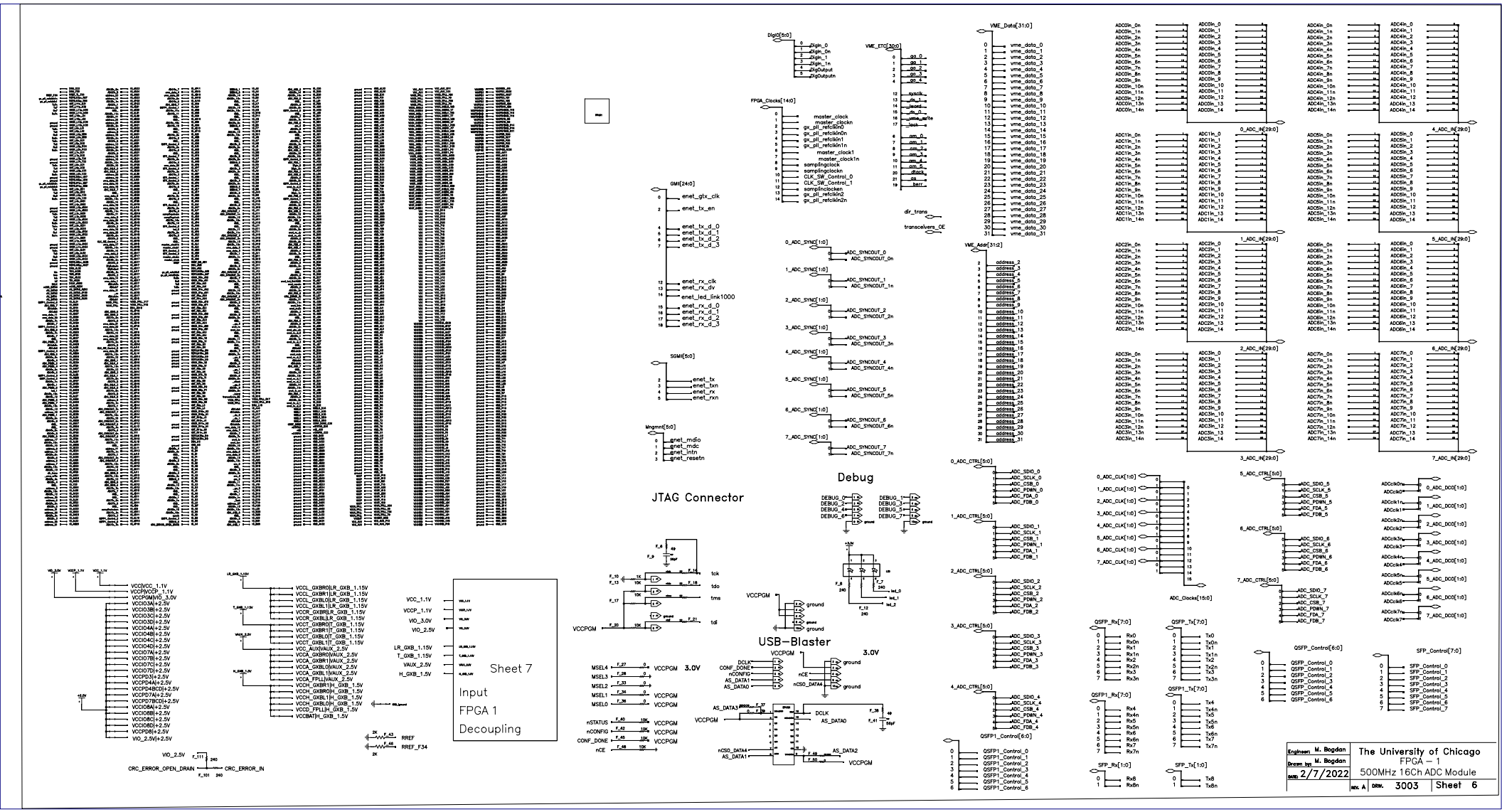
JTAG Connector
Debug
USB–Blaster
Sheet 7
Input
FPGA 1
Decoupling
ADC_Clocks[15:0]
The University of Chicago
FPGA – 1
500MHz 16Ch ADC Module
Engineer: M. Bogdan
Drawn by: M. Bogdan
DATE: 2/7/2022
REV. A
DRW. 3003
Sheet 6