Preliminary 30ns Shaper vs. 45 ns Shaper Simulation Results

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This note presents preliminary simulation results for the front end electronics for the J-Parc-K Experiment. The simulations were performed on two circuits: the existing 3-in-1 card, which was designed for about 45ns width at half height and a new shaper designed for 30 ns width at half height. The schematics are presented in Figure 1.

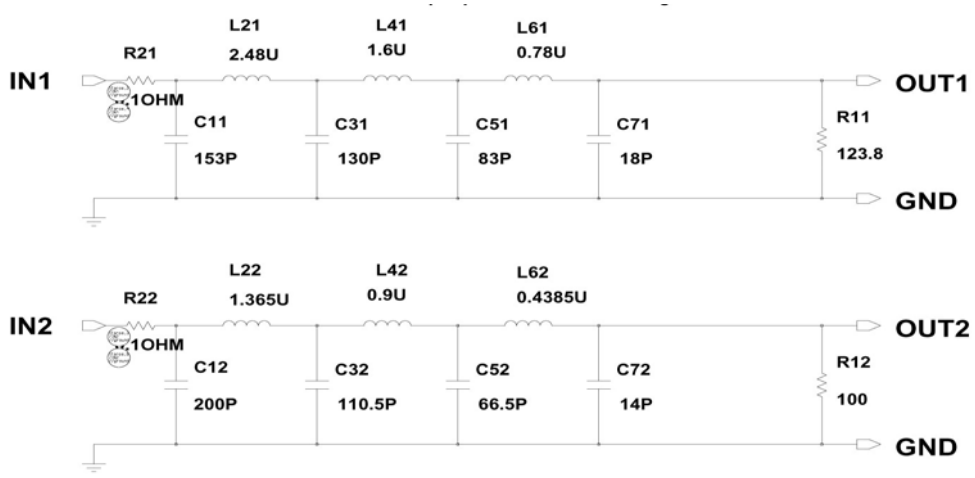

Figure 1. Test circuits: IN1 - 45ns shaper (the 3in1 card), IN2 - 30ns shaper.

The simulation results are presented in Figure 2. The simulation shows that for our input pulse, the 30ns shaper's falling edge becomes so long that the total width at half-height is about 42ns, just about the same as for the 45ns shaper but with a much worse symmetry.

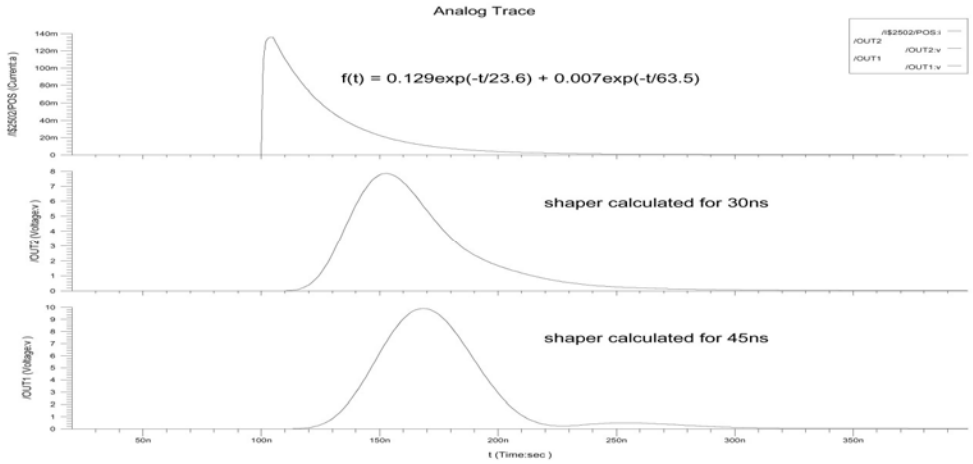

Figure 2. Simulation Results