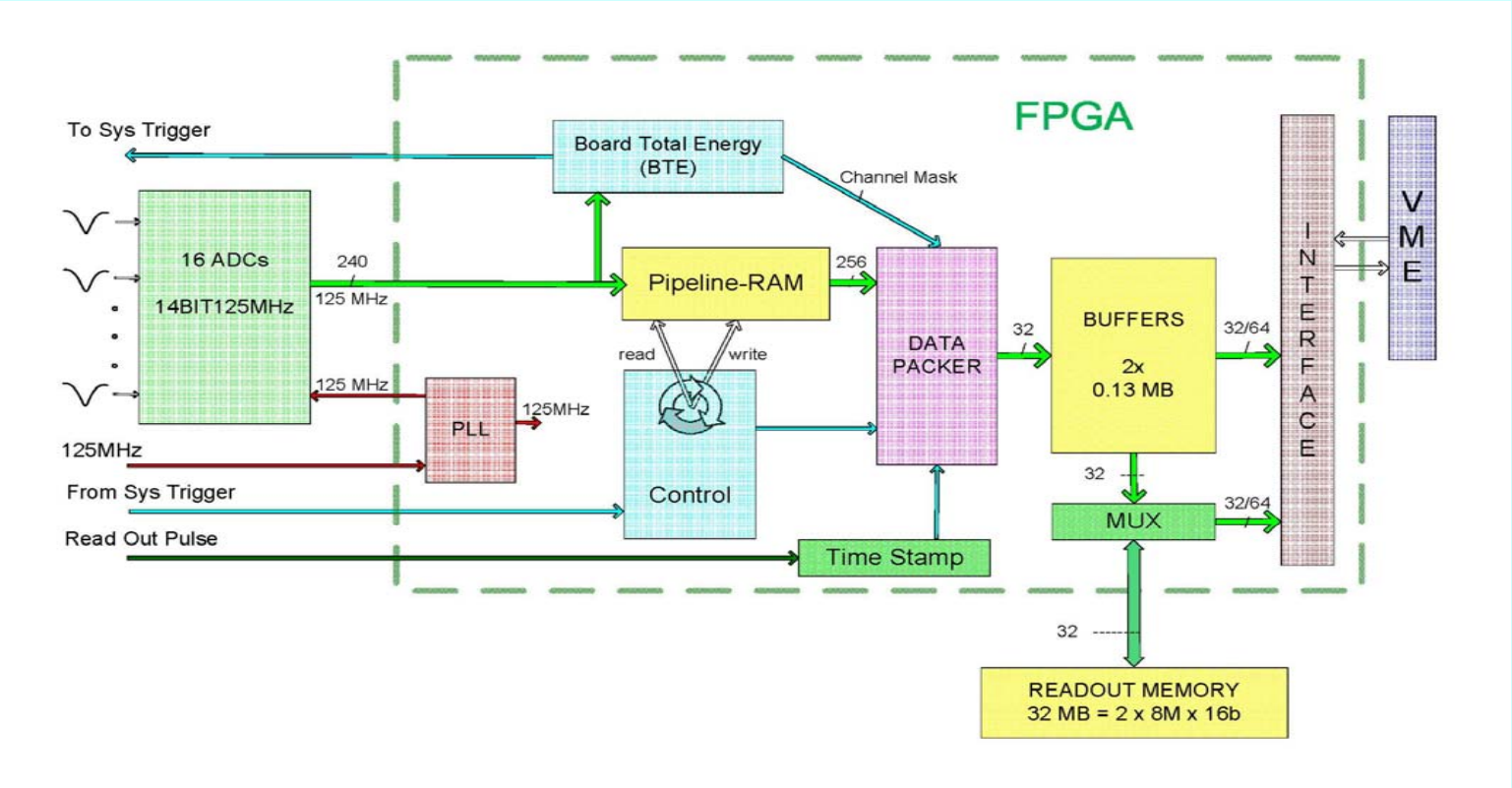
14-BIT Custom ADC Board Rev. B

The University of Chicago

Block Diagram

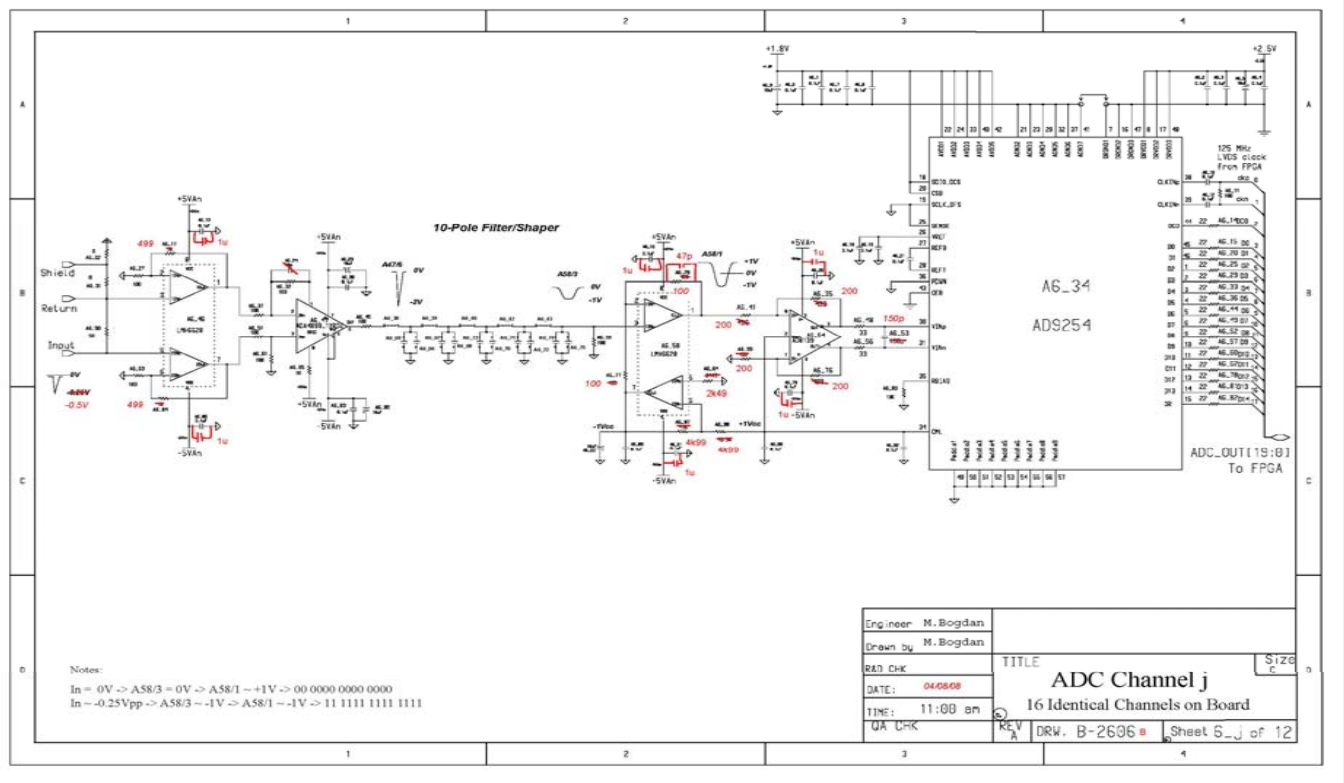


Same Block Diagram + Readout Memory outside FPGA (32 Mbytes):

- Input Pipeline: ~4us depth (512 samples);
- Two buffers inside FPGA – 4096 words each;
- 40kHz trigger, 100% hit occupancy, 32 samples/trigger (256ns), 32bytes/sample;
- Readout Memory (2 x MT45W8MW16BGX) can store 0.75 second spill.

Shaper/ADC Channel

Revision B Schematic



Noise STDEV Rev. A:

2.80 LSB – Dec.'07 FNAL recordings – full chain;

2.65 LSB – EShop recordings – ADC Module alone.

Module SNR ~ 70dB

Noise STDEV Rev. B (ADC Module alone):

1.90 LSB – same signal shape/bandwidth;

1.70 LSB – more signal filtering just before A/D chip –> pulse ~5% wider.

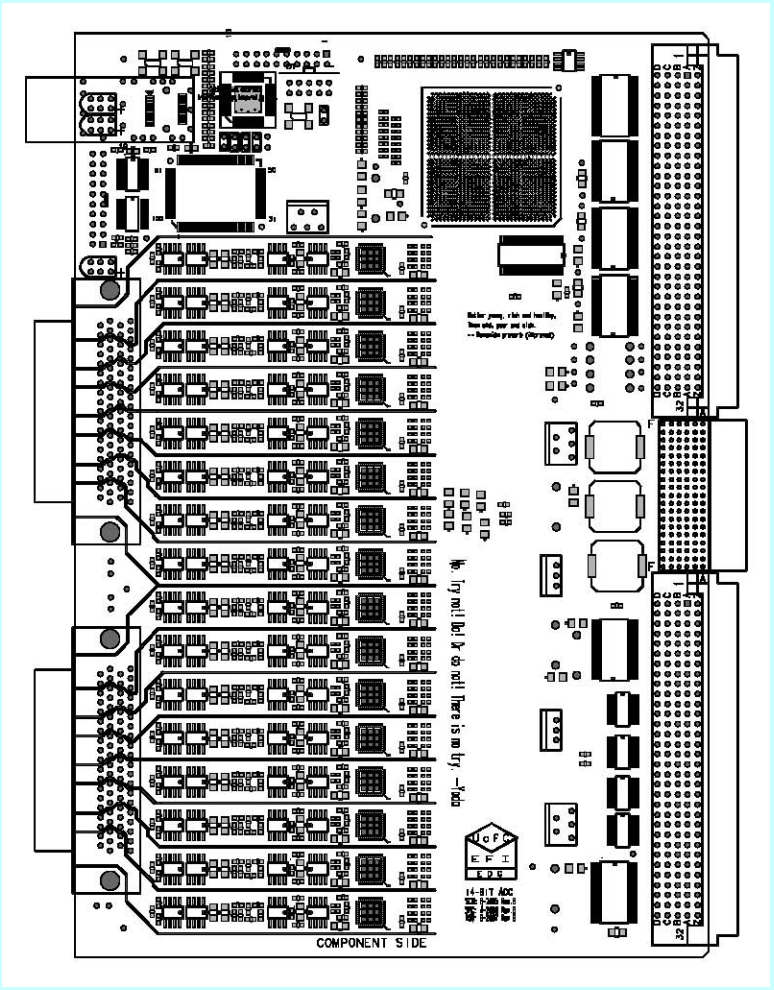
Module SNR ~73-74dB

Note: SNR was calculated as: RMS Full-scale/STDEV Noise.

PCB Layout

Crosstalk related Modifications:

- Increase channel spacing by 1mm;
- Use 2 connectors - 8 channels each;
- Fully split power planes between channels from connectors to ADC chips;
- Use smaller size, shielded inductors for the shapers;
- Provide solder pads for individual channel shielding (if needed).



Layout – Preliminary (memory not included).

Specifications

- Digital I/Os (non VME)

  Backplane:
  - 16-BIT parallel outputs on P2/J2 – for ET Sum;
  - 4 diff bused lines on P0/J0 - for sampling clock and trigger pulses (VIPA Crate Only!);

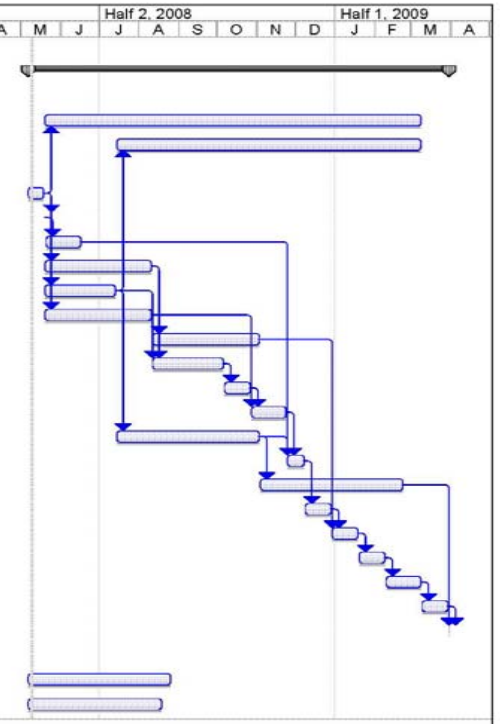
  Front Panel:
  - 4 LVDS inputs – optional for sampling clock and trigger pulses;
  - Optical Link – optional;

- Power Requirements:

  +5V – 2A;
  +3.3V – 4.7A;
  -5V – 1.25A (applied on the user defined –V1,V2 pins);
  The +/-12V power pins are not used any more.

Schedule

ID	Task Name	Duration	Start	Finish	Cost
1					
2	**ADC Rev.B for 100-Channel Test**	**235 days**	**Wed 5/7/08**	**Tue 3/31/09**	**$169,500.00**
3					
4	Engineering - 1 person	210 days	Tue 5/20/08	Mon 3/9/09	$126,000.00
5	Software & Firmware Design - (Postdoc/Student)	170 days	Tue 7/15/08	Mon 3/9/09	$0.00
6					
7	ADC Module Rev. B Specifications Finish	9 days	Wed 5/7/08	Mon 5/19/08	$0.00
8	Test Cable Specification Finish	1 day	Tue 5/20/08	Tue 5/20/08	$0.00
9	Design & Manufacture 4-pc. Test Cable Assy.	20 days	Wed 5/21/08	Tue 6/17/08	$500.00
10	Schematic Design Rev.B	60 days	Tue 5/20/08	Mon 8/11/08	$0.00
11	Basic Firmware Modifications	40 days	Tue 5/20/08	Mon 7/14/08	$0.00
12	Order Components for 2pc. Module	60 days	Tue 5/20/08	Mon 8/11/08	$4,000.00
13	Order Components for 10pc Module	60 days	Tue 8/12/08	Mon 11/3/08	$20,000.00
14	Board Layout, Simulation	40 days	Tue 8/12/08	Mon 10/6/08	$0.00
15	Manufacture 3 pc. PCB Rev.B	15 days	Tue 10/7/08	Mon 10/27/08	$3,000.00
16	Assembly 2-pc Module	20 days	Tue 10/28/08	Mon 11/24/08	$3,000.00
17	Firmware & Software Design for In-House Test	80 days	Tue 7/15/08	Mon 11/3/08	$0.00
18	Test Module and Cable in Huse	10 days	Tue 11/25/08	Mon 12/8/08	$0.00
19	Firmware & Software Design for 100-Channel Test	80 days	Tue 11/4/08	Mon 2/23/09	$0.00
20	Manufacture 10pc. PCB Rev. B	15 days	Tue 12/9/08	Mon 12/29/08	$5,000.00
21	Assembly 2pc Module - First Item	15 days	Tue 12/30/08	Mon 1/19/09	$3,000.00
22	Test 2- pc. First Item in House	15 days	Tue 1/20/09	Mon 2/9/09	$0.00
23	Assembly 8 pc. Module	20 days	Tue 2/10/09	Mon 3/9/09	$5,000.00
24	Test 8pc. Module in House	15 days	Tue 3/10/09	Mon 3/30/09	$0.00
25	ADC Modules and Cables Ready for 100-Channel Test	1 day	Tue 3/31/09	Tue 3/31/09	$0.00
26					
27	**Purchase 1 pc. Crate for testing in house**	**80 days**	**Wed 5/7/08**	**Tue 8/26/08**	**$9,000.00**
28	**Manufacture 20pc. Cable (Cable Min Order: 2,500 ft)**	**75 days**	**Wed 5/7/08**	**Tue 8/19/08**	**$22,000.00**



Project: ADC_RevB_Schedule.mpp
Date: Fri 5/9/08

Task
Split
Progress
Milestone
Summary
Project Summary
External Tasks
External MileTask
Split

Page 1

Self Trigger Method

Implement a block inside FPGA (No Hardware Change):

- Calculate board total energy over last 32 samples, generate “board energy value” every 8 ns.
- Do on-the-fly fitting of each channel, generate a “board fitting accuracy value” every 8 ns.
- The two values produce self trigger. (May trigger at larger that 8ns increments.)
- Create self triggered “board event”.
- Time stamp (8 ns increments) in the header word for each board event.
- Off line, each board event gets associated, and aligned with the others.
- Generate "system event", and discard junk.

How much junk (board events not part of system events) is recorded?

- Simulation may answer that.

This method could be tested during the 100-channel test, and compared with the triggered solution.

- May prove itself useful for other applications.