14-BIT Custom ADC Board

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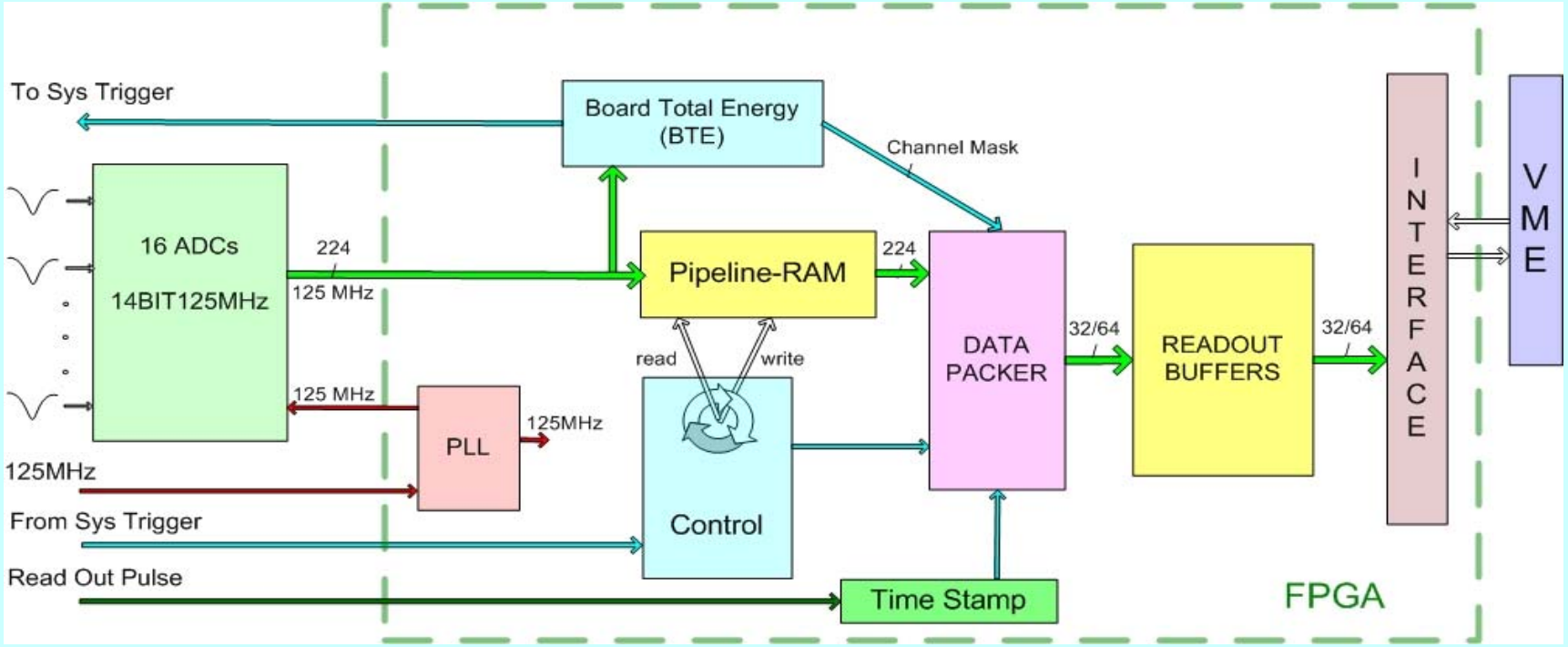
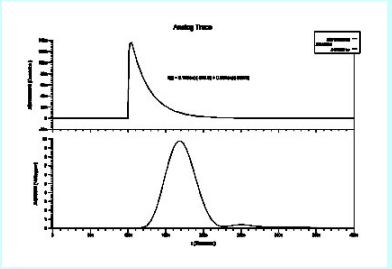
14-Bit, 125MHz ADC Board – Block Diagram



- **Each ADC channel - one AD9254 chip: 14 bits/125MHz;**
- **7-Pole Filter/Shaper Included on Board;**
- **One STRATIX II FPGA EP2S60F1020 for 16 ADC channels:**
  - **Trigger rate: 10kHz, 32 samples/trigger (256ns);**
  - **Input Pipeline: ~25us depth (3,200 samples);**
  - **Two VME readout buffers - max 128 triggers, (10 ms);**
- **Optical Link with: TLK2501, V23829-N305-B57 (can be stuffed if needed).**



Schematic – Top Level

Front Panel LVDS Inputs*:

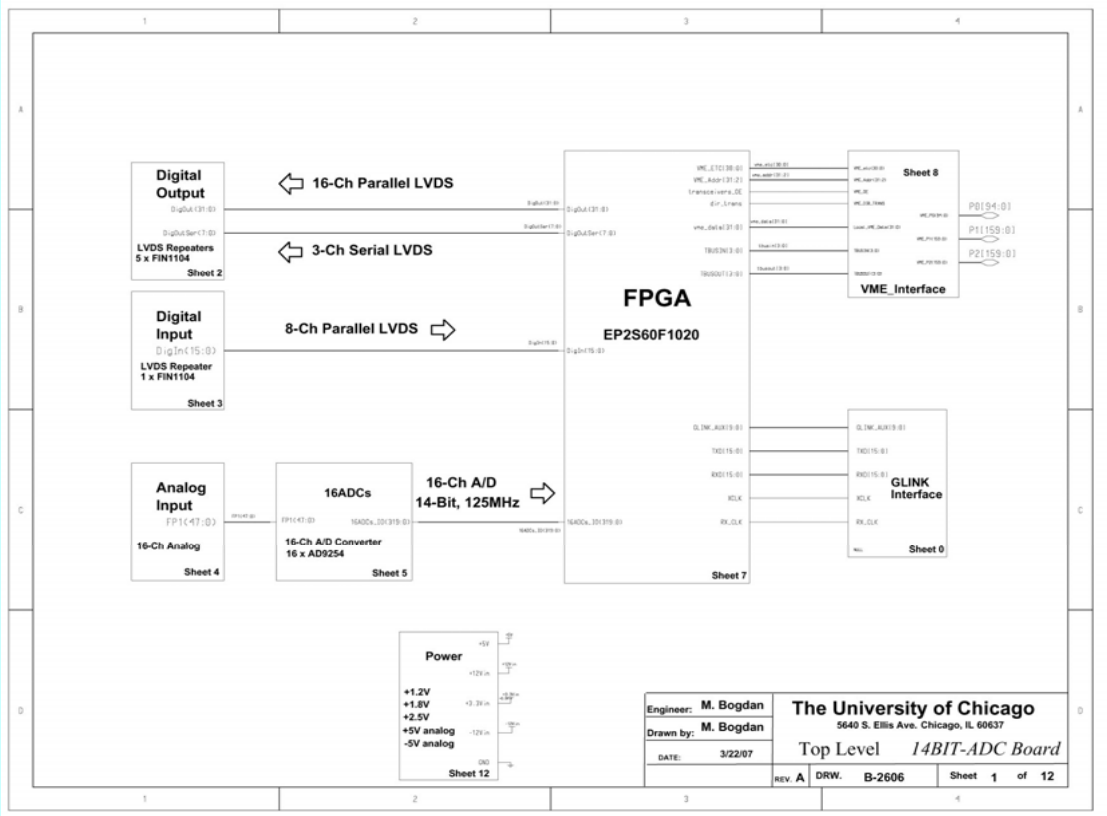
- **8-Bit Parallel:**
  - **Sys clock, triggers from TS;**

Front Panel LVDS Outputs*:

- **16-Bit Parallel, 12-Bit Serialized:**
  - **Board Energy Info to TS;**

Readout:

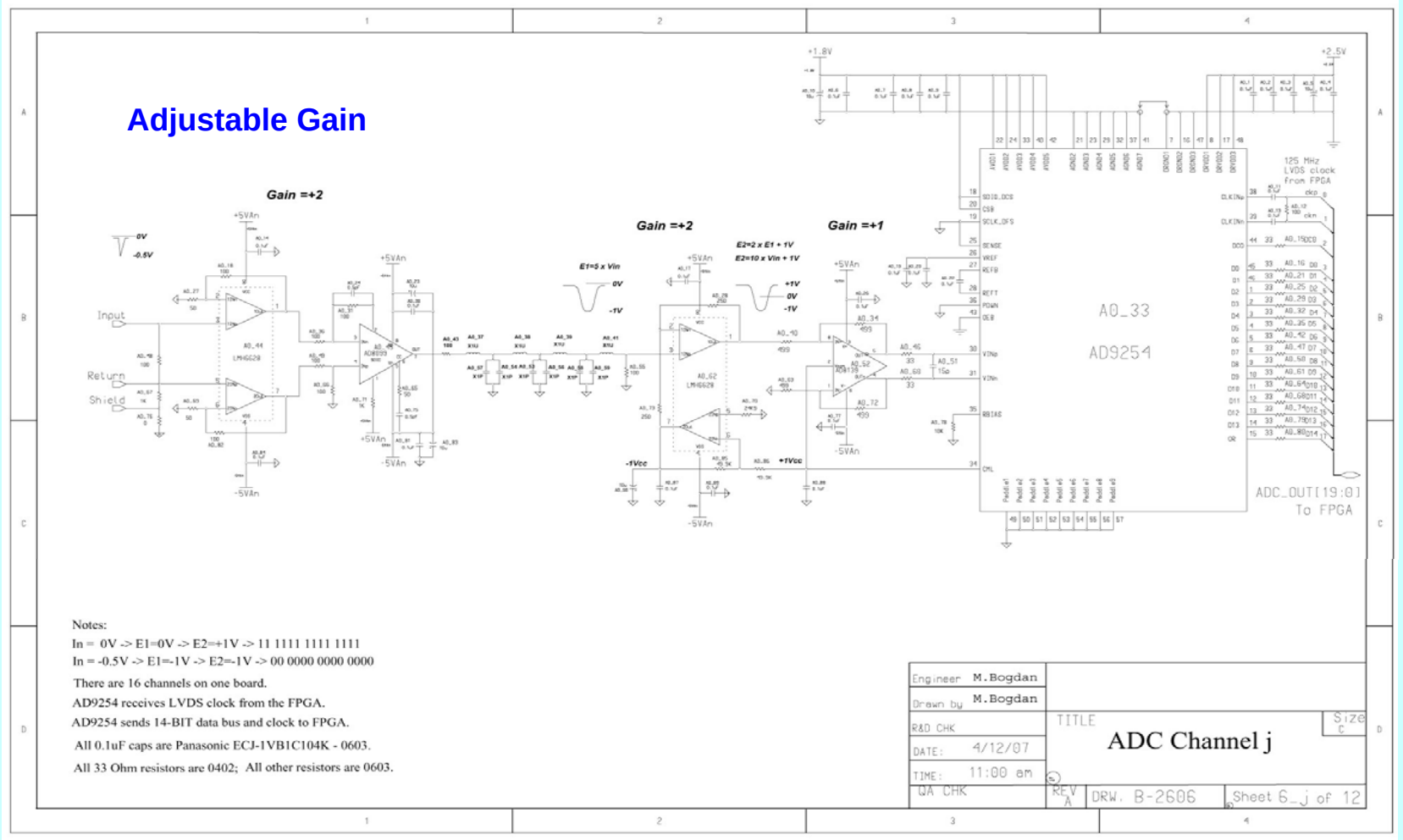
- **VME32/64 with CBLT;**
- **GLINK/SLINK if needed.**



Actual Board schematic – DA/Mentor Graphics

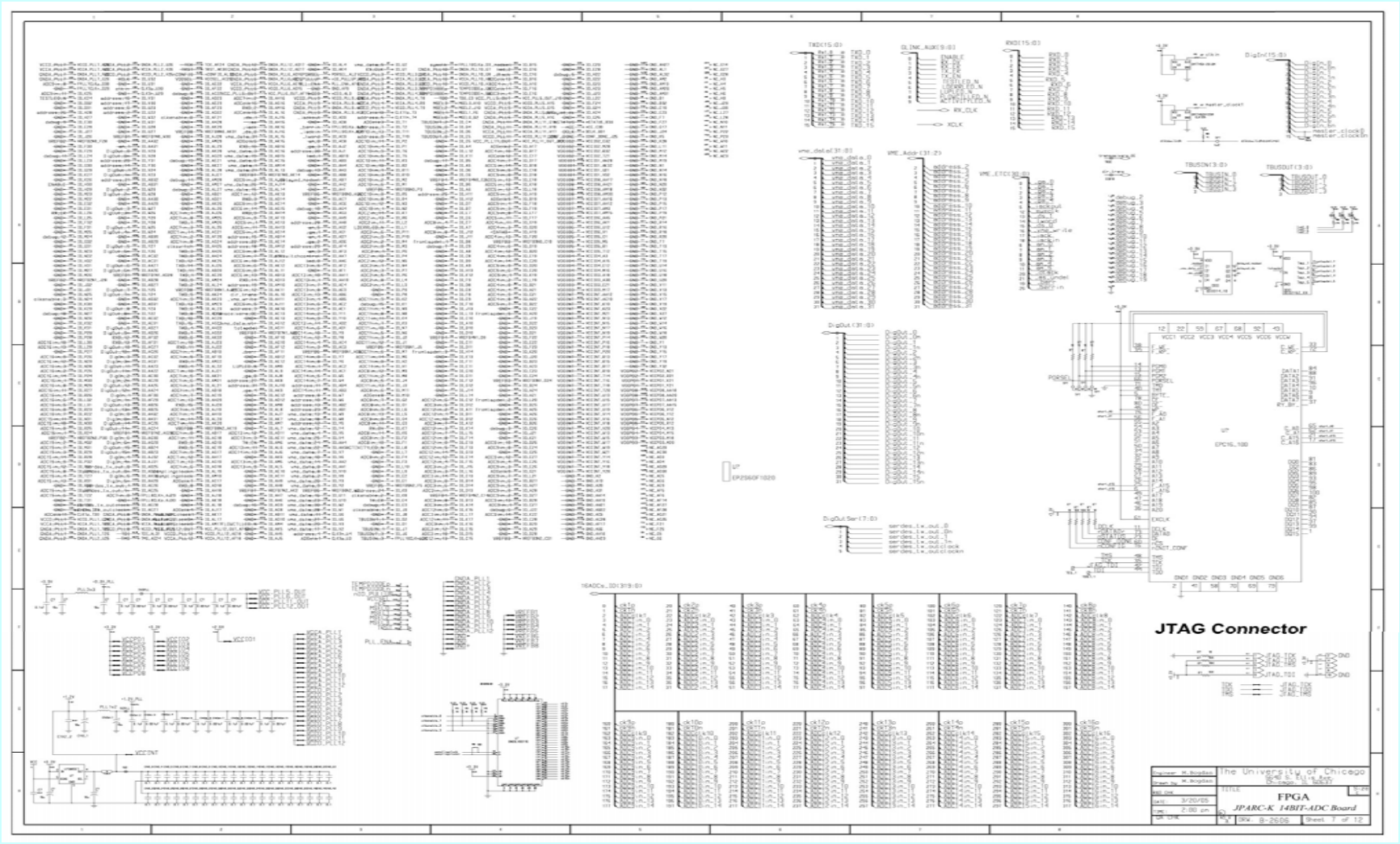
(*) Comments regarding the number of I/O Bits are welcome.

Schematic – Shaper/ADC Channel



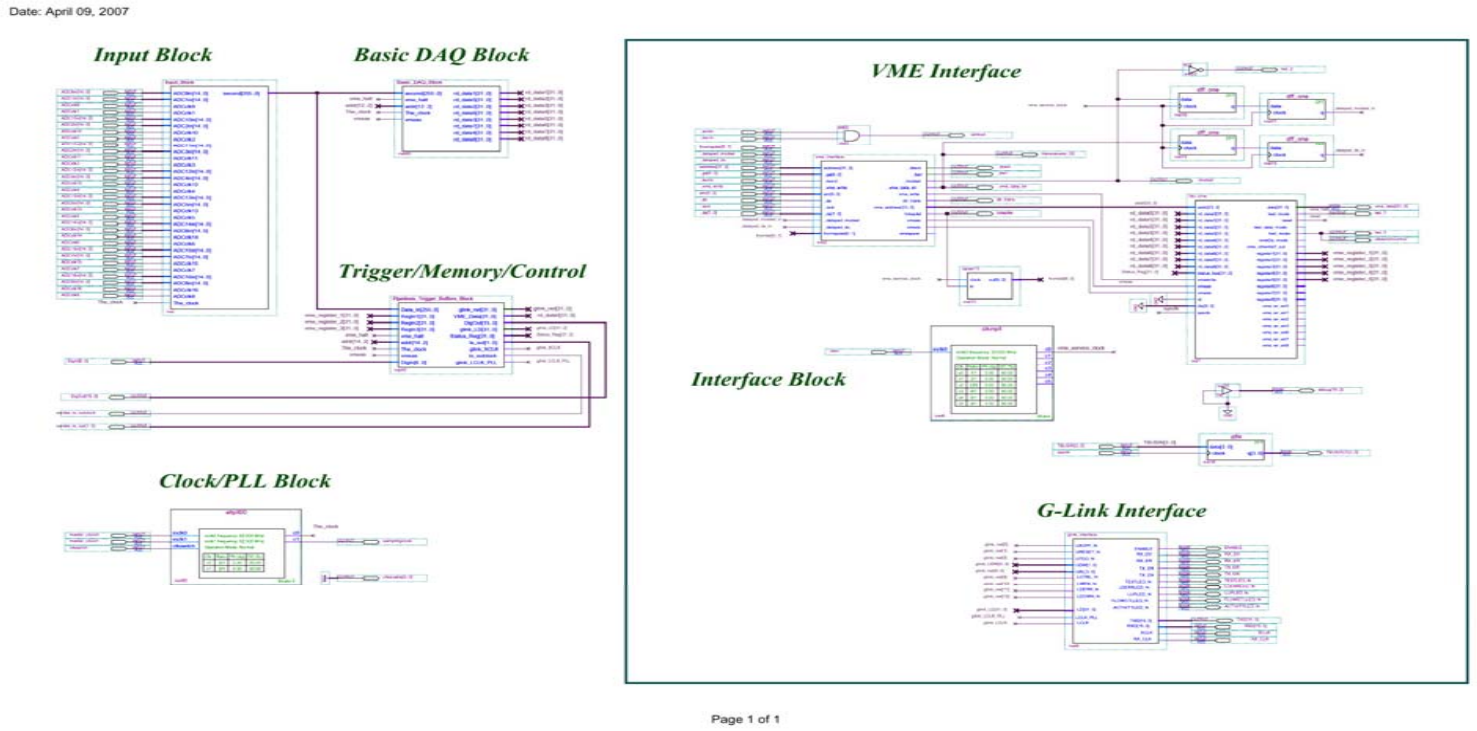
Actual Board schematic – DA/Mentor Graphics

Schematic – FPGA Block



Actual Board schematic – DA/Mentor Graphics

Altera Project – Block Diagram



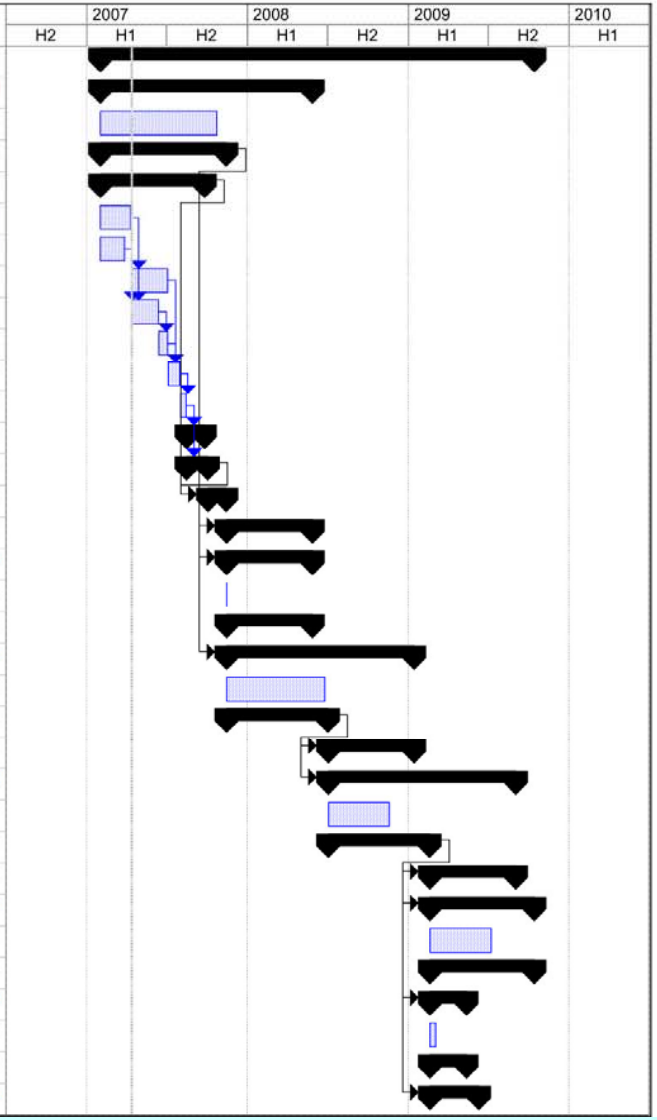
Actual Basic FPGA Design – Altera Quartus

Design is sufficient for beam test only: can record, store, and read out 3,200 samples/25us.

To Do: **- Trigger/Memory/Control block (BTE calculator, Pipeline, Data Packer, Control, etc.);**
- G-Link Interface – if needed.

Schedule

ID	Task Name	Duration	Start	Finish	Cost
1	**J-PARC K - DAQ System**	**705 days**	**2/2/07**	**10/15/09**	**$1,552,440.00**
2	**Csl-DAQ 3,200Ch/200Bds: 14BIT,125MHz,16Ch/Bd**	**345 days**	**2/2/07**	**5/29/08**	**$685,600.00**
3	**Engineering 1 person**	190 days	2/2/07	10/25/07	$121,600.00
4	**Prototype Test-Fermilab - 16 Channels**	**205 days**	**2/2/07**	**11/15/07**	**$24,000.00**
5	**14BIT,125MHz,16Ch ADCs Prototype**	**170 days**	**2/2/07**	**9/27/07**	**$22,000.00**
6	**Schematic Design - Finished**	50 days	2/2/07	4/12/07	$0.00
7	**Basic Firmware Design - Finished**	40 days	2/2/07	3/29/07	$0.00
8	**Order Components**	60 days	4/13/07	7/5/07	$6,000.00
9	**Board Layout, Simulation**	45 days	4/13/07	6/14/07	$0.00
10	**Manufacture PCB**	15 days	6/15/07	7/5/07	$3,000.00
11	**Assy. Prototype**	20 days	7/6/07	8/2/07	$4,000.00
12	**Test Prototype in Huse**	10 days	8/3/07	8/16/07	$0.00
13	**Rev. B - if needed**	**30 days**	**8/17/07**	**9/27/07**	**$9,000.00**
17	**Test Setup**	**35 days**	**8/17/07**	**10/4/07**	**$2,000.00**
22	**Testing at Fermilab**	**30 days**	**10/5/07**	**11/15/07**	$0.00
25	**Production - 200 pc ADC-125 Boards**	**140 days**	**11/16/07**	**5/29/08**	**$540,000.00**
30	**Veto-DAQ 512Ch/32Bds: 14BIT,125MHz,16Ch/Bd**	**140 days**	**11/16/07**	**5/29/08**	**$87,040.00**
31	**Engineering (Same design as Csl-DAQ)**	1 day	11/16/07	11/16/07	$640.00
32	**Production - 32 pc ADC-125 Boards**	**140 days**	**11/16/07**	**5/29/08**	**$86,400.00**
37	**BHPV-DAQ 100Ch/25 Bds: 12BIT, 500MHz,4Ch/Bd**	**305 days**	**11/16/07**	**1/15/09**	**$258,900.00**
38	**Engineering 1person**	160 days	11/16/07	6/26/08	$102,400.00
39	**12BIT,500MHz,4Ch FADCs Prototype**	**165 days**	**11/16/07**	**7/3/08**	**$34,000.00**
53	**Production -25 pc 4-Ch FADC-500 Boards**	**140 days**	**7/4/08**	**1/15/09**	**$122,500.00**
58	**Crate Traffic Controller (CTC) Board**	**305 days**	**7/4/08**	**9/3/09**	**$131,500.00**
59	**Engineering 1person**	100 days	7/4/08	11/20/08	$64,000.00
60	**CTC Board Prototype**	**165 days**	**7/4/08**	**2/19/09**	**$24,000.00**
74	**Production -15 pc CTC Boards**	**140 days**	**2/20/09**	**9/3/09**	**$43,500.00**
79	**System Trigger Module (STM)**	**170 days**	**2/20/09**	**10/15/09**	**$88,000.00**
80	**Engineering 1person**	100 days	2/20/09	7/9/09	$64,000.00
81	**Production 2-3 pc STM Board**	**170 days**	**2/20/09**	**10/15/09**	**$24,000.00**
95	**Cables**	**60 days**	**2/20/09**	**5/14/09**	**$76,400.00**
96	**Engineering 1person**	10 days	2/20/09	3/5/09	$6,400.00
97	**Production**	**60 days**	**2/20/09**	**5/14/09**	**$70,000.00**
99	**VME Crates w/Power Supplies**	**80 days**	**2/20/09**	**6/11/09**	**$225,000.00**



Conclusions

- **Good simulation results on PreAmp/Shaper schematic and FPGA design;**
- **Have to proceed now with the prototype;**