# Custom 14-Bit, 125MHz ADC/Data Processing Module for the KL Experiment at J-Parc

Mircea Bogdan, Jiasen Ma, Harold Sanders, Y. Wah

***Abstract*–We present a custom 16-Channel ADC/Data Processing Module, designed for a high energy physics kaon experiment at JPARC (Japan Particle Accelerator Research Complex). This Board will receive signals from the Cesium Iodide (CsI) Calorimeter, and will be one of the two ADC Modules in the Experiment's DAQ System. Each analog PMT pulse is amplified and passed through a 10-pole filter/shaper, before being applied to a 14-Bit, 125MHz sample-and-hold ADC chip. Sampling for all 3,200 calorimeter channels is simultaneous on one low jitter system clock. Data are then processed locally with Field Programmable Gate Arrays (FPGAs) that perform the board total energy calculation and determine real-time energy related values for the System Trigger Supervisor. These values are presented in both parallel and serialized formats on the front panel. The module is provided with a pipeline, up to 25us (3,200 samples) long, which stores the acquisitions, awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. The readout can be performed via the VME32/64 backplane, or via the front panel optical link.**

## I. Introduction

THE paper presents a custom 16-Channel, 14-Bit, 125 MHz, ADC/Data Processing Module, designed for the Step 1 of a kaon Experiment E14 [1] at JPARC. E14 is an International High Energy Physics Experiment to study CP Violation, at the new Japanese Accelerator Complex.

## II. Implementation

The E14 Experiment's Data Acquisition System is presented in Fig. 1. It consists of three major blocks:

- The Cesium Iodide (CsI) DAQ Block – with up to 2,816 Channels of 14Bit/125 MHz ADCs, in 11 Crates;
- The Veto DAQ Block – with up to 512 Channels of 14Bit/125 MHz ADCs, in 2 Crates;
- The Beam Hole Phase Veto (BHPV) DAQ Block – with up to 100 Channels of 12Bit/500MHz ADCs, in 4 Crates.

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M. Bogdan is with The University of Chicago, Chicago, IL 60637 USA (telephone: 773-834-8483, e-mail: bogdan@edg.uchicago.edu).

J. Ma is with The University of Chicago, Chicago, IL 60637 USA (telephone: 773-702-3483, e-mail: jsma@hep.uchicago.edu).

H. Sanders is with The University of Chicago, Chicago, IL 60637 USA (telephone: 773-702-7801, e-mail: harold@edg.uchicago.edu).

Y. Wah is with The University of Chicago, Chicago, IL 60637 USA (telephone: 773-702-7592, e-mail: ywah@uchicago.edu).

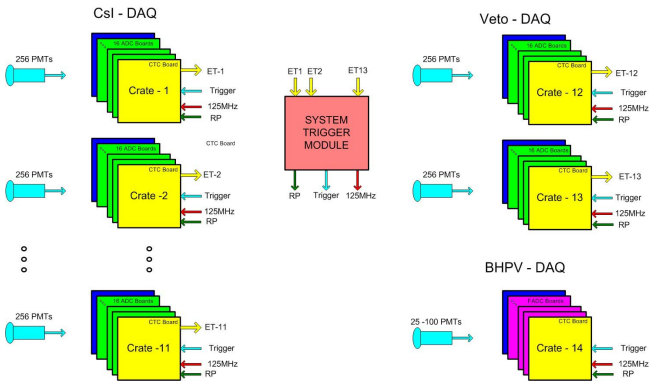


Fig.1. The E14 Data Acquisition System. The full system is implemented in three DAQ Blocks: The Cesium Iodide DAQ, the Veto DAQ, and the Beam Hole Phase Veto DAQ.

Each DAQ Block will be configured in 6U VME Crates. The CsI and the Veto DAQ Blocks will use the same ADC Hardware Modules, loaded with different firmware implementations. The BHPV DAQ will use different, 12-Bit, 500 MHz ADC Boards.

All Modules work on a common sampling clock, provided by the System Trigger Supervisor (STS) Module, along with the trigger and the readout synchronization pulses. All these signals are sent to the entire system, and passed along to the ADC boards via the custom Crate Traffic Controller (CTC) Modules located one in each crate. The block diagram of a crate in the CsI and Veto DAQ Blocks is presented in Fig. 2.

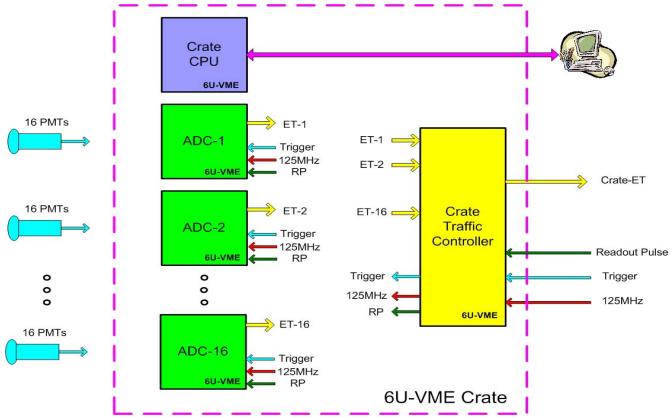


Fig. 2. Block diagram of a crate in the CsI and Veto DAQ Blocks. Each crate includes 16 ADC Modules, one Crate Traffic Controller Module, and one Crate CPU.

The Crate Traffic Controller Board will work as interface between the System Trigger Supervisor and each individual

ADC Module, to insure simultaneous sampling and readout. Communication is done via LVDS front-panel lines.

The ADC/Data Processing Module has 16 analog channels. The schematic of one of these channels is presented in Fig. 3.

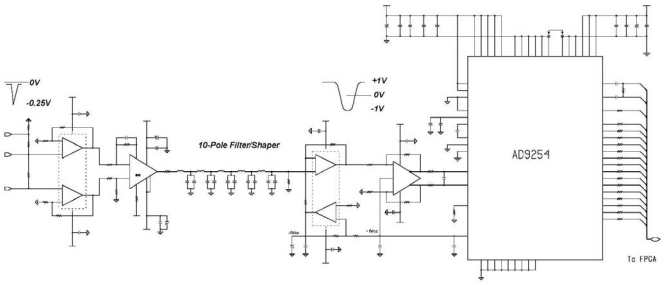


Fig. 3. Schematic of the analog channel, including the input buffer, the 10-pole filter/shaper, and the A/D converter. There are 16 such identical channels on the ADC Board.

The input signal (250mVpp – full scale) comes directly from one of the Calorimeter's Photomultiplier Tubes (PMT), and goes first to a buffer (Gain~10; Zi=100Ohm), implemented with an LMH6628 in a typical differential configuration. The signal is then passed on to a 10-pole Bessel filter/shaper and is converted into Gaussian form, while keeping the total energy information constant. The filter was calculated for optimal Full Width at the Half-Height (FWHH) of the resulting Gaussian shape, with respect to fitting and timing.

Fig. 4 presents preliminary simulation results of an analog PMT signal, being applied to the 10-pole filter on board, with 45ns FWHH.

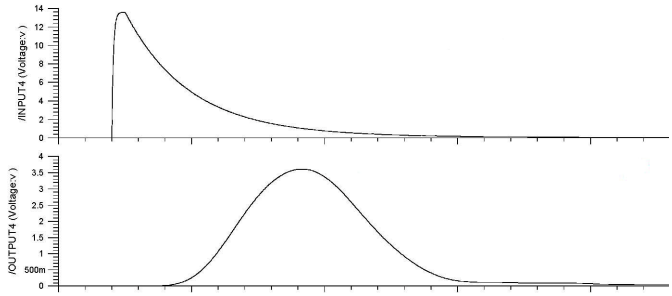


Fig. 4. Simulation of an analog input signal from the CsI-PMT, which is passed through the 10-pole filter/shaper. The filter converts the narrow PMT pulse, and gives it a Gaussian shape with optimal FWHH.

After shaping, the analog pulse is applied to the ADC chip via an AD8139 differential driver. The ADC chip AD9254 works at 125MSPS, with continuous parallel data reading.

The board's logic is presented in the block diagram in Fig. 5. The digitized data are processed locally with a Field Programmable Gate Array (FPGA) EP2S60F1020C5, from the Altera Stratix II family [2] that performs the Total Board Energy calculation and determines real-time energy related values for the STS. These values are presented in both parallel and serialized formats on the front panel.

The module is provided with an adjustable pipeline 3,200 samples long, which stores the acquisitions, awaiting the system trigger pulse. This insures a digital data delay of up to 25us. After a trigger, sets of data are packed and buffered for continuous readout, with no dead time.

There are two readout buffers implemented, holding a maximum of 128 triggered acquisitions, with 32 samples each (256 ns). Considering a trigger rate of about 10 kHz, each buffer can hold up to 10ms worth of data. The readout can be performed via the VME32/64 backplane, or via the front panel optical link.

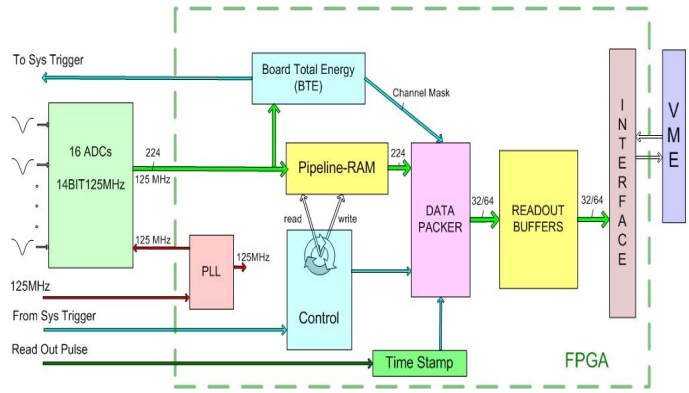


Fig. 5. FPGA Design – Block Diagram

## III. Conclusions

This ADC/Data Processing module was designed to accommodate the particular requirements for the CsI Calorimeter in the J-Parc KL Experiment, such as:

- 3,200 channels of 14-Bit sample-and-hold ADCs with simultaneous sampling at rates up to 125MHz;
- Signal conditioning with 10-pole filters, that convert the analog narrow signals from the PMTs into Gaussian shaped pulses with optimal FWHH;
- Low input noise: ~35uVrms (250 mV input range);
- Powerful real-time processing capabilities within the on board FPGA, to perform the total board energy calculation. The high-density Altera Stratix II device allows for future design or algorithm modifications.
- Relatively small size (6U VME for 16 channels).

At this time, two prototypes are manufactured and tested.

## References


[1] E14: Proposal for $K^0_L \rightarrow \pi^0 \nu\nu$ Experiment at JPARC, approve July 2007.

[2] Altera Corporation, Stratix II Device Handbook, v.2.1., May 2007.