

14BIT 125MHz ADC Board

Power Test

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Testing of the FPGA Core Supply for the 14-BIT 125MSPS ADC Module

Problem:

Compressed Data transmission between the ADC Boards and L2 shows RX errors occurring in L2, in sync with the L1 Accept pulses.

The errors were traced back to the ADC Modules, i.e. to temporary voltage drops in the VCCINT=1.2V power supply feeding the FPGA's core and PLL blocks.

Testing of the FPGA Core Supply for the 14-BIT 125MSPS ADC Module

Firmware Simulations with the Quartus Power Analyzer Tool showed current consumption of over 2A for the core VCCINT.

Core VCCINT Current depends on:

- Number of Logic Cells Used
- Clock frequency
- Toggle Rate - we simulated with 12 to 15% (clock =100%)

For this FPGA, I_{VCCINT} can change from 400mA to over 3A, depending on design complexity.

For the Beam Test Designs I_{VCCINT} was between 600mA to 800mA.

VCCINT is supplied by a 3A LDO.

Current Measurement

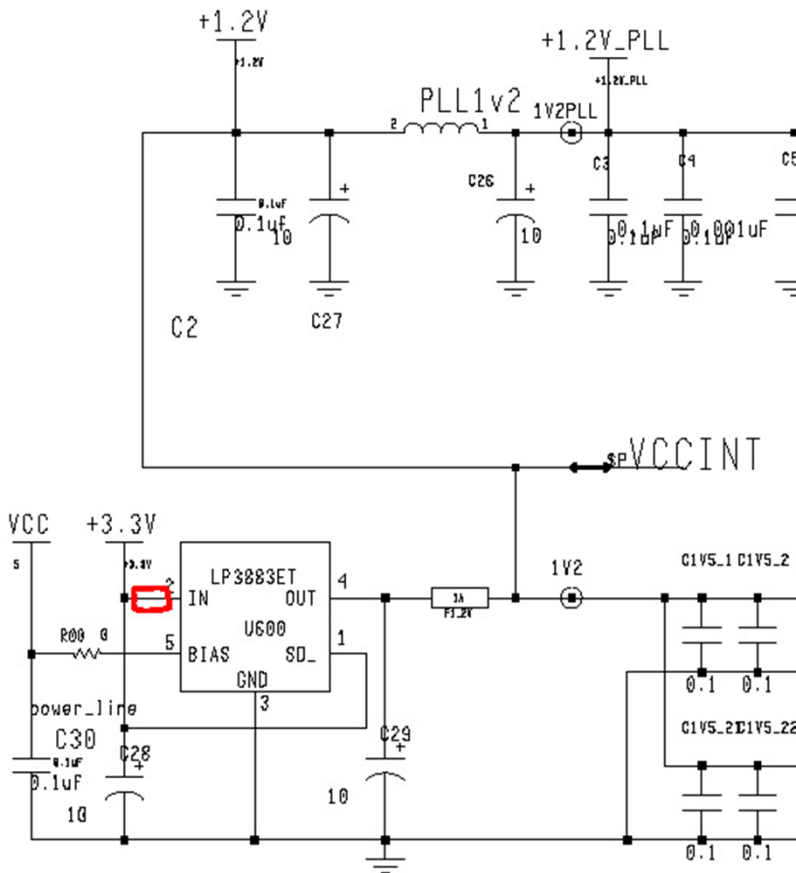
L1A pulse every 64us, LIVE=1.

Method 1.

Amp Meter instead of Fuse showed ~1.4A with compression active or not (simulation was showing between 2 and 3A with compression, depending on toggle rate).

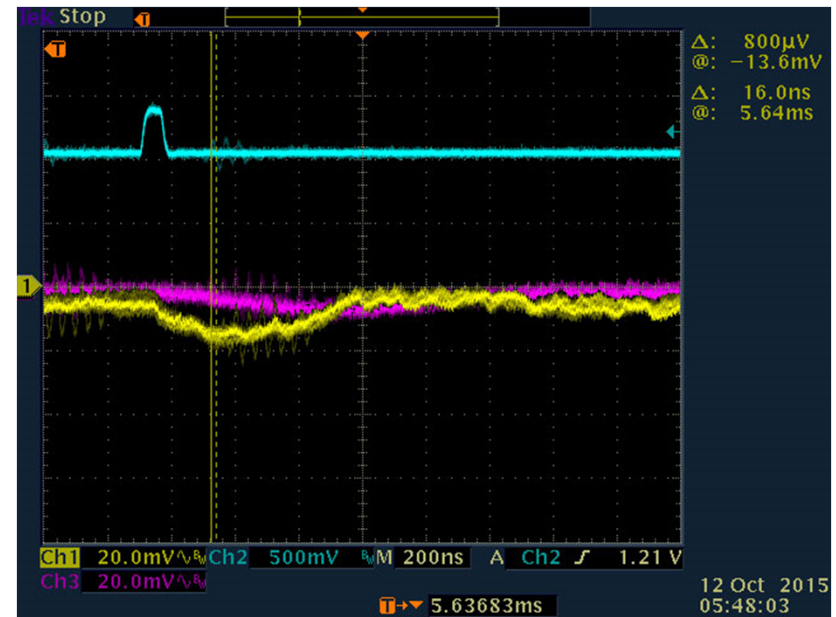
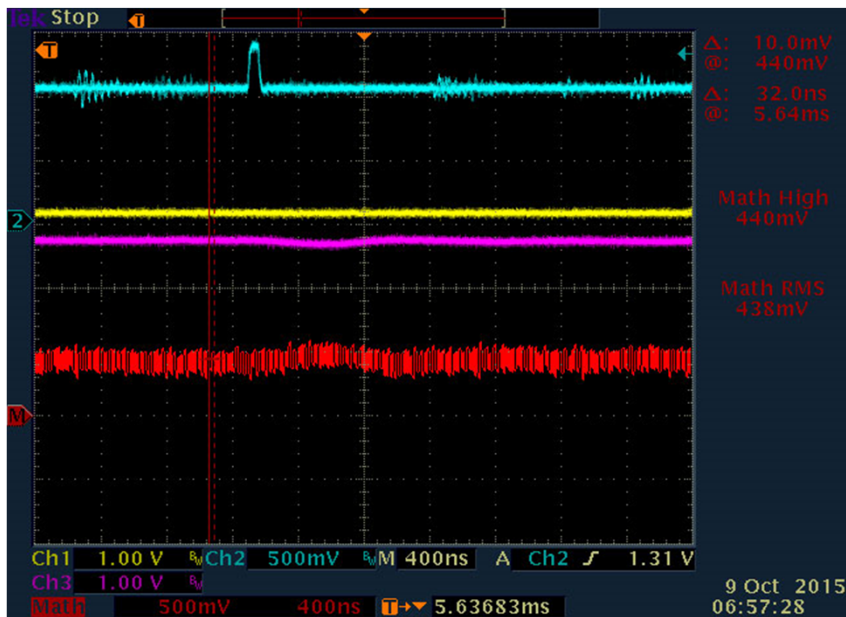
Method 2.

We measured Voltage Drop across a 300mOhm series resistor, in sync with a L1A pulse.



Current/Voltage Test Compression OFF

(v2071.sof – pedestals at ADC inputs)



Channel 2 = L1A pulse

Channels 1,3 = Voltage on test resistor

Math(Ch1 - Ch3) $\Rightarrow I_{VCCINT} = 1.46A_{RMS}$

With data compression inactive, the FPGA core current has a small temporary increase, corresponding to FPGA internal data processing which follows a L1A pulse.

Channel 2 = L1A pulse

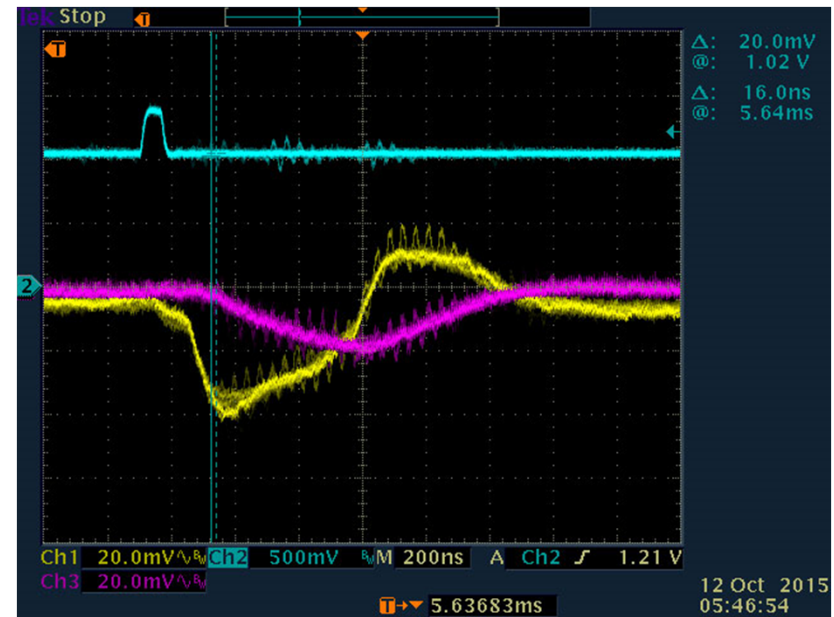
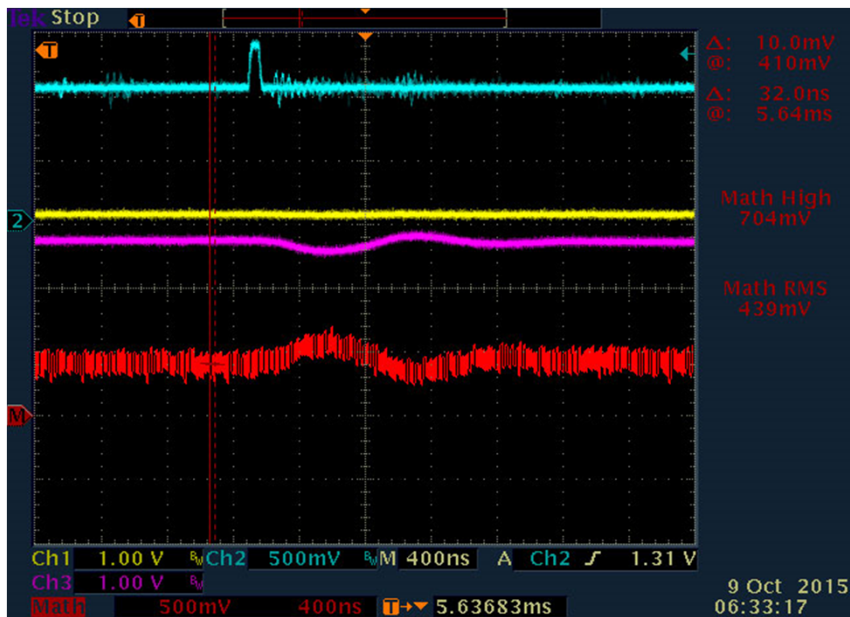
Channel 1 = VCCINT = 1.2Vcc

Channel 3 = +1.2V_PLL = 1.2Vcc filtered

These voltage drops are causing no noticeable problems in FPGA functionality.

Current/Voltage Test Compression ON

(v2071.sof – pedestals at ADC inputs)



Channel 2 = L1A pulse

Channels 1,3 = voltage on test resistor

Math(Ch1 - Ch3) $\Rightarrow I_{VCCINT} = 1.463A_{RMS}$

With data compression active, the FPGA core current has temporary increases of up to 2.3A, corresponding to FPGA internal data processing which follows a L1A pulse.

Channel 2 = L1A pulse

Channel 1 = VCCINT = 1.2Vcc

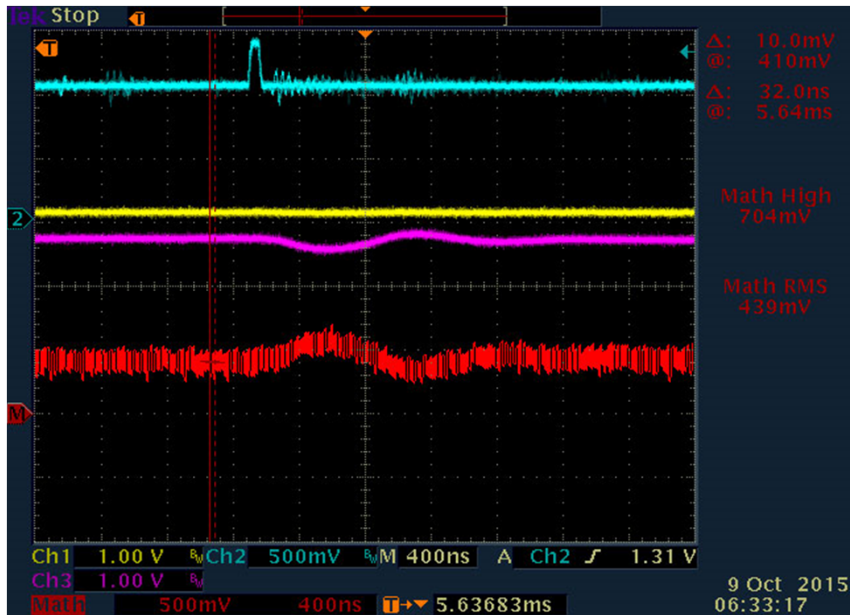
Channel 3 = +1.2V_PLL = 1.2Vcc filtered

The recommended minimum value for VCCINT and +1.2V_PLL is 1.15V

These Voltage drops are still OK or borderline, since Rx errors occur only when pulses are applied, i.e. toggle rate is increased.

Current/Voltage Test Compression ON

(v2071.sof – pedestals at ADC inputs)

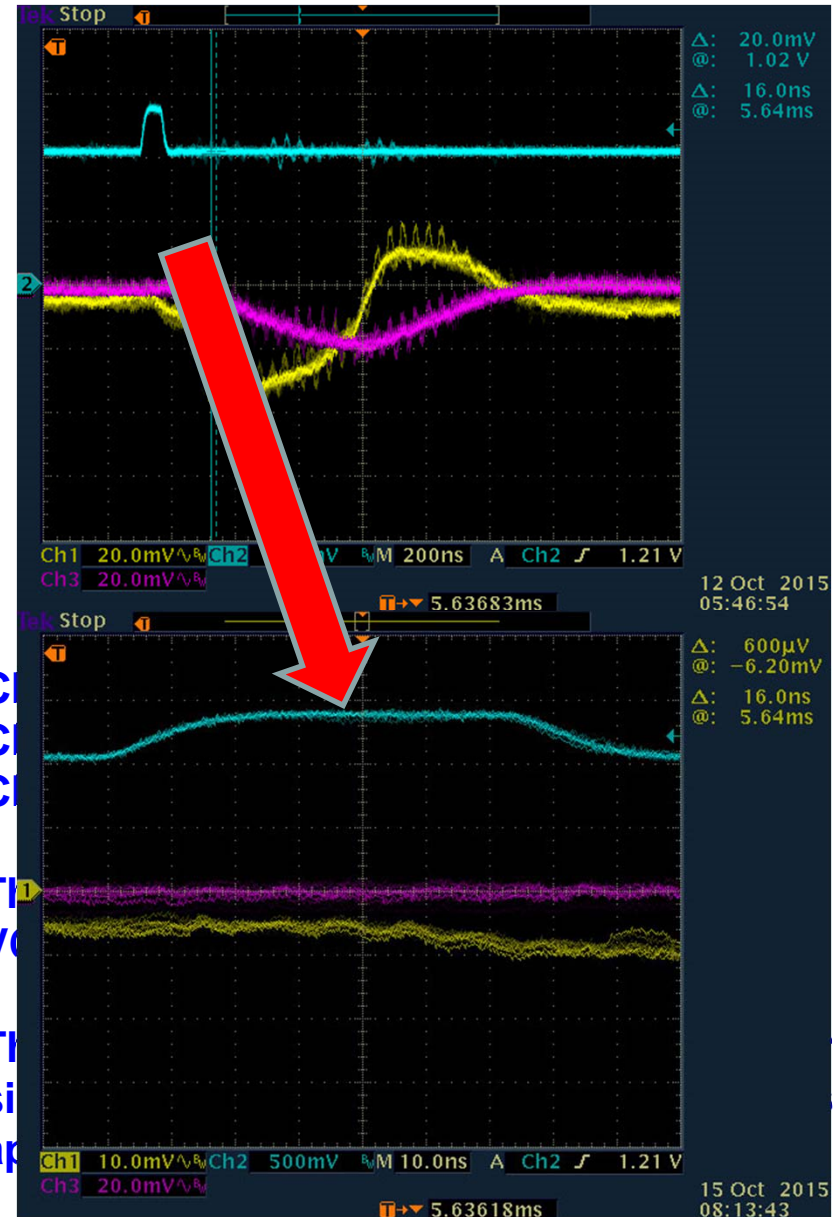


Channel 2 = L1A pulse

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With data compression active, the FPGA core current has temporary increases of up to 2.3A, corresponding to FPGA internal data processing which follows a L1A pulse.



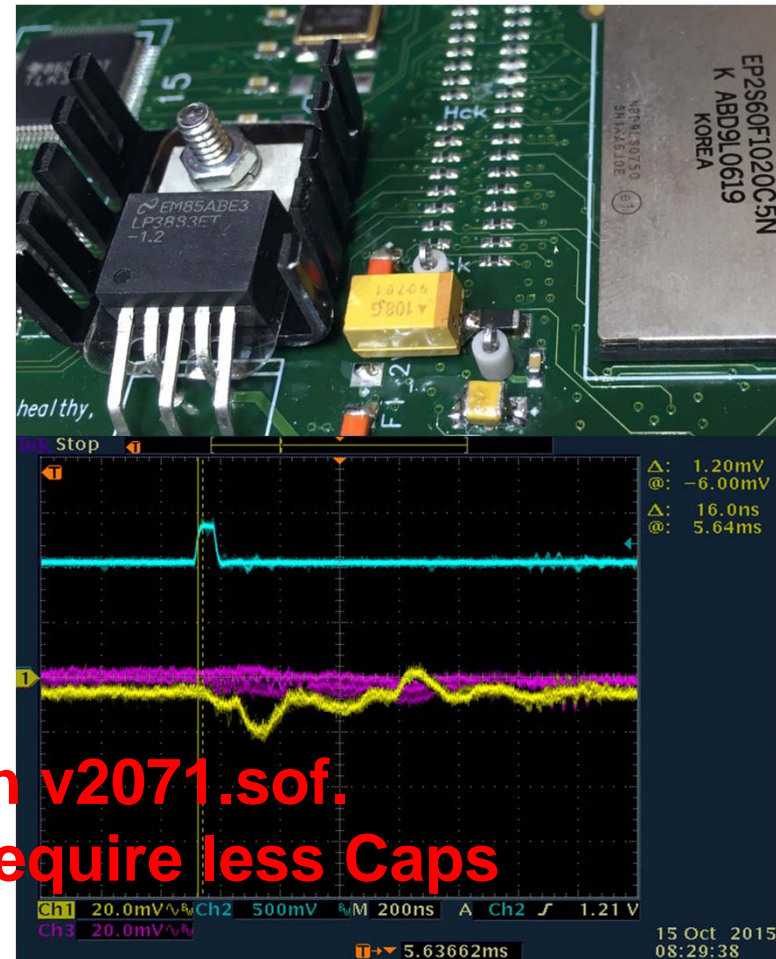
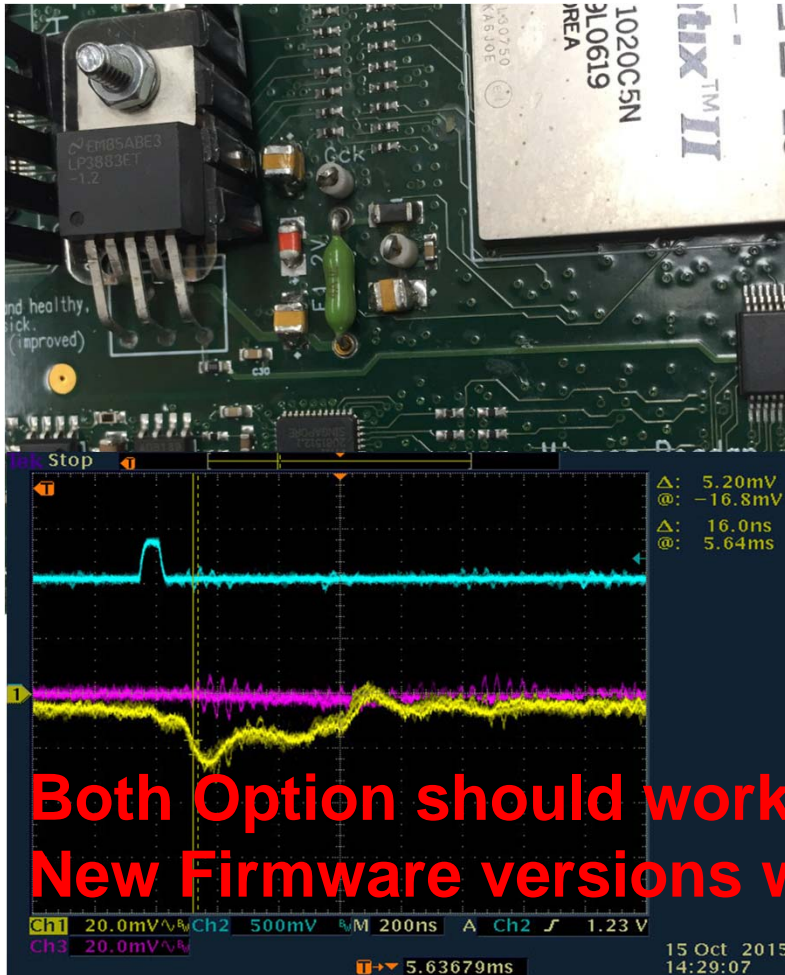
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Voltage Test with different C26, C27

2+1+1 - 470uF caps

(v2071.sof – pedestals at ADC inputs) 1,000uF x 470uF caps



Replacing C26, C27 from 10uF to 470uF or larger shows improvement of VCCINT and +1.2V stability during the brief intervals of increased demand.

Combination Firmware/Hardware has to be optimized – WORK IN PROGRESS