Preliminary Front End Analog Simulation Results for J-Parc-K Electronics

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This note presents preliminary simulation results for the front end electronics for the J-Parc-K Experiment. The simulations, 10 in total, were performed on an existing circuit; the 3-in-1 card designed by UC-EDG for the ATLAS Experiment.

The part of the schematic I used, was the input filter/shaper, witch is actually a 7-pole, low-pass filter with the cutoff frequency of about 12.8MHz.

The input pulses are exponential: f(t)= 0.129exp(-t/23.6) + 0.007exp(-t/63.5). Each simulation has two pulses: a full pulse and an additional pulse 20% in amplitude. As the plots below present, the additional pulse comes before or after the full pulse.

The complete simulation files can be found at:
http://edg.uchicago.edu/~bogdan/jparc_k/misc/3in1sim_results.zip

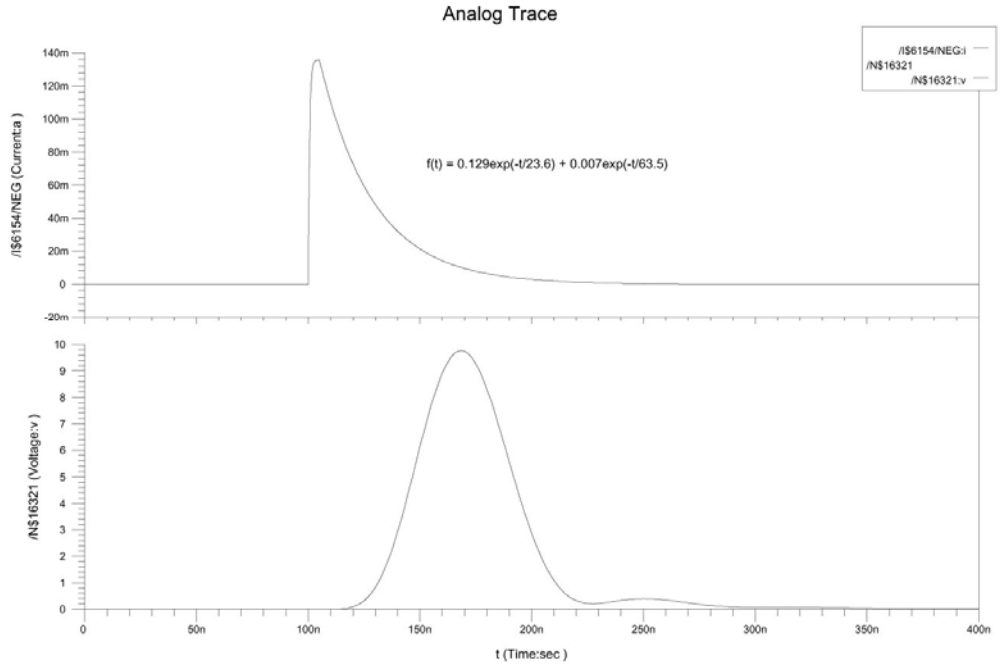

Figure 1. One single pulse.

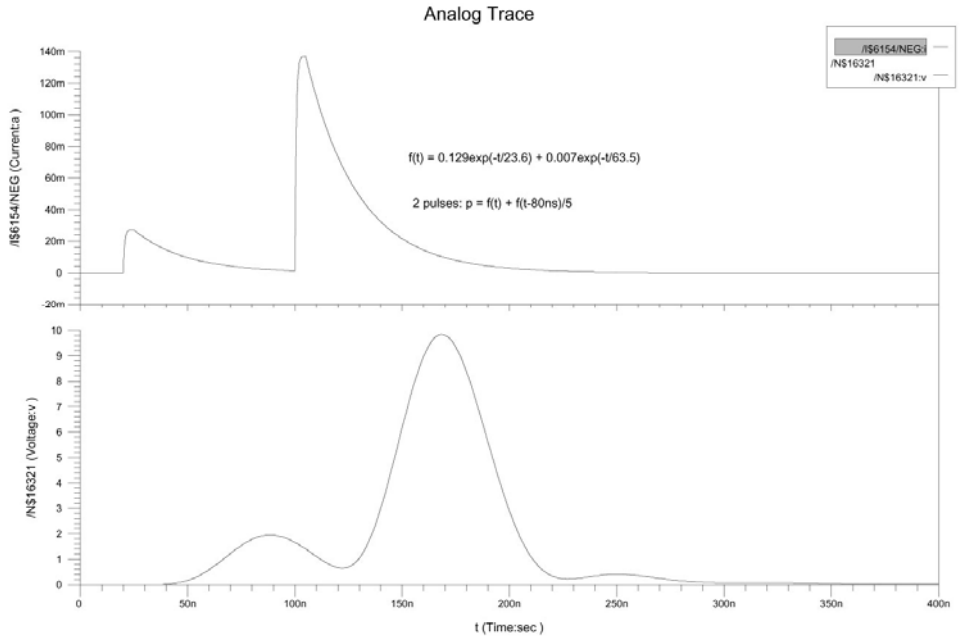

Figure 2. Two pulses - the additional pulse is 80ns before the full pulse.

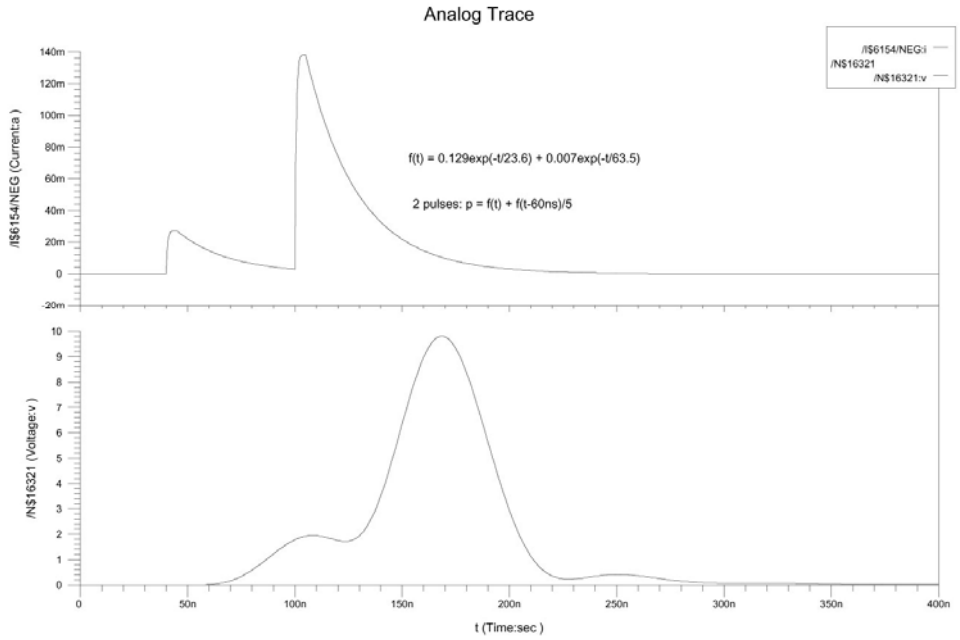

Figure 3. Two pulses - the additional pulse is 60ns before the full pulse.

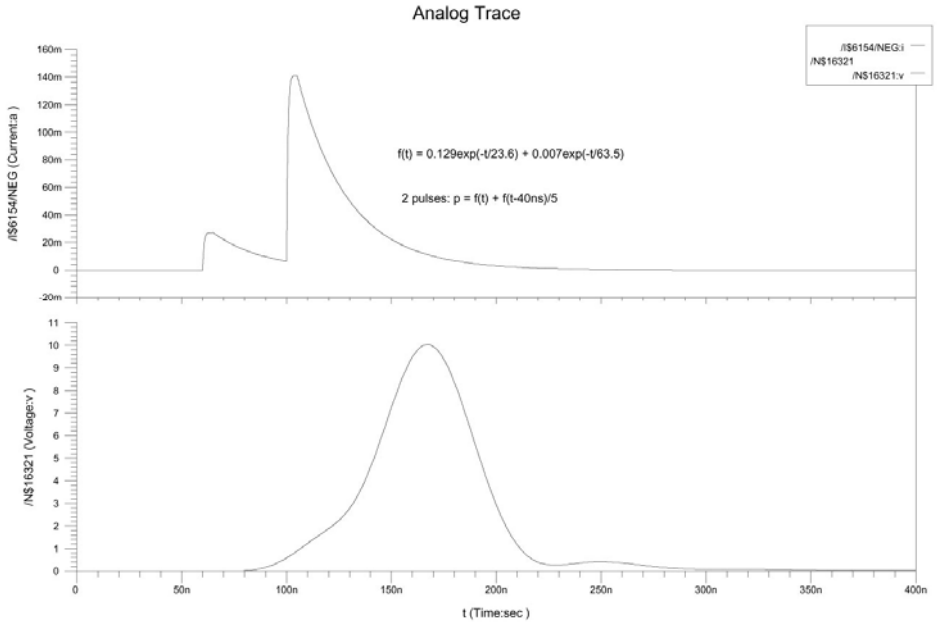

Figure 4. Two pulses - the additional pulse is 40ns before the full pulse.

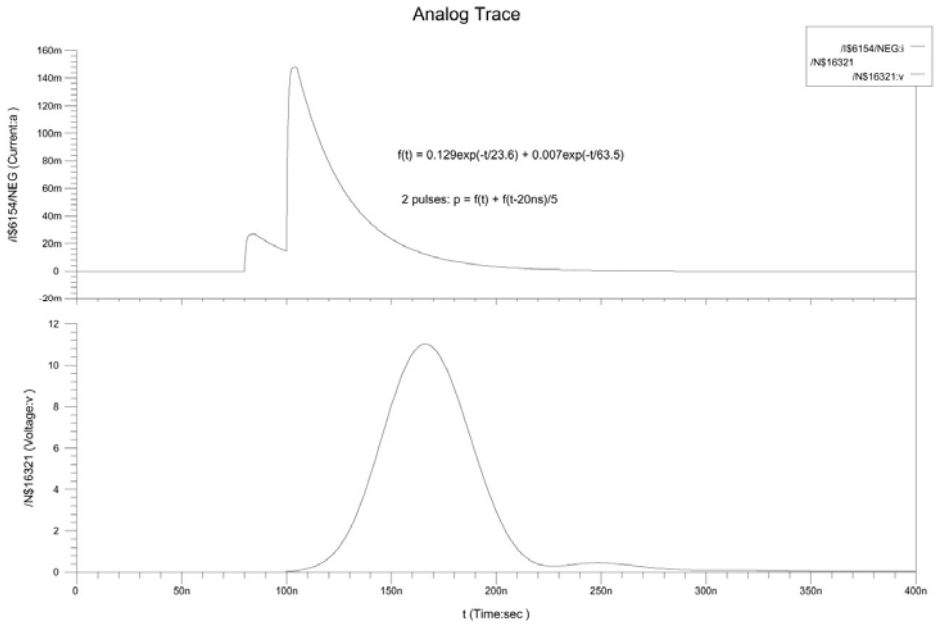

Figure 5. Two pulses - the additional pulse is 20ns before the full pulse.

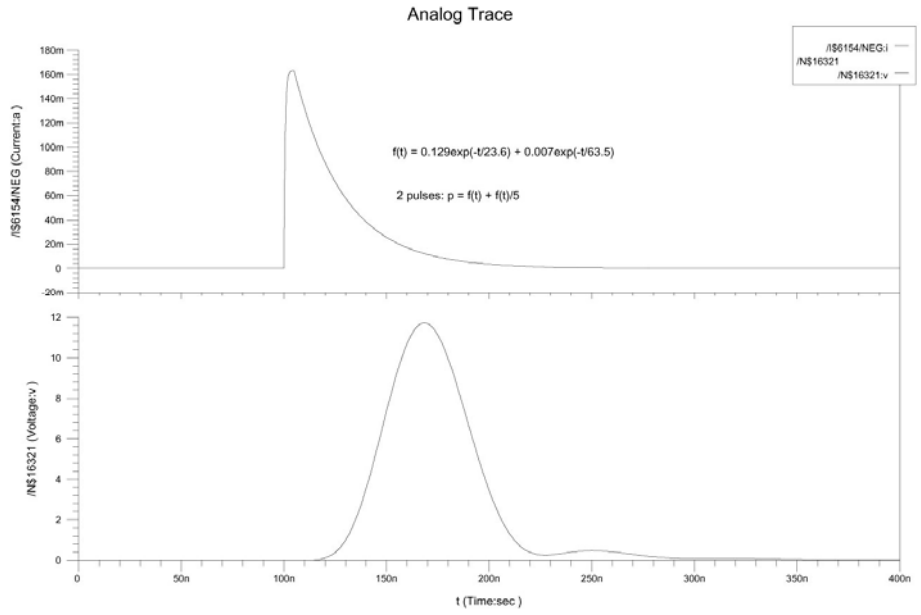

Figure 6. Two pulses - the additional pulse is overlapped with the full pulse.

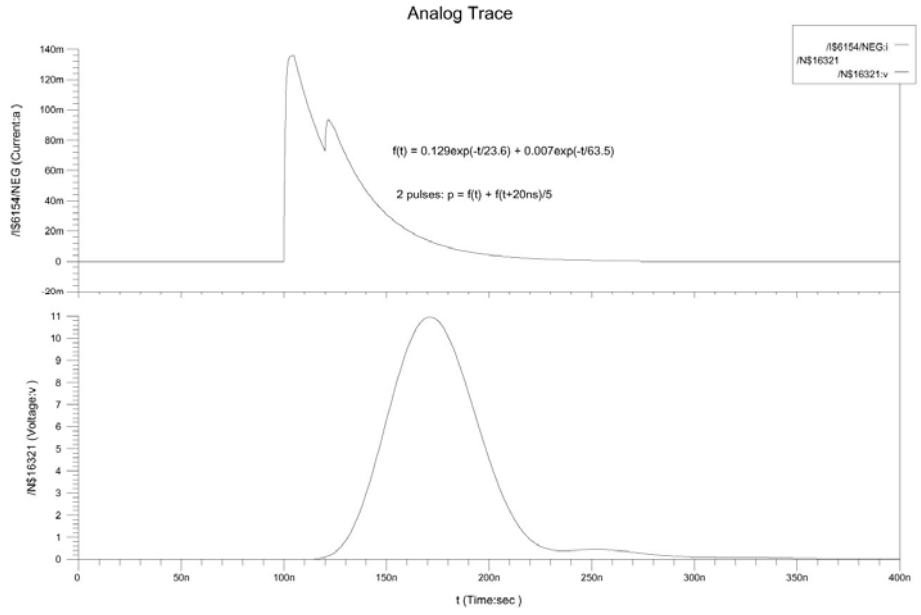

Figure 7. Two pulses - the additional pulse is 20ns after the full pulse.

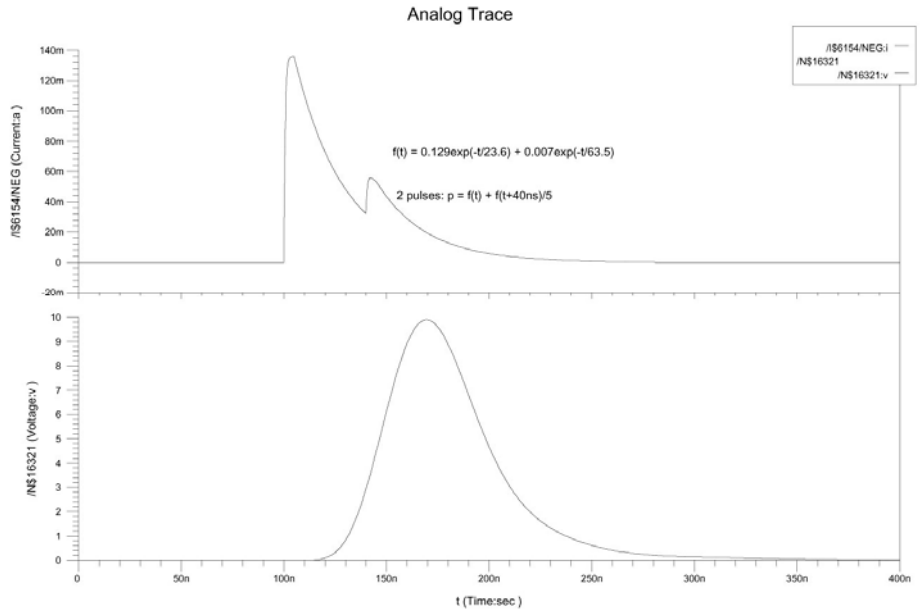

Figure 8. Two pulses - the additional pulse is 40ns after the full pulse.

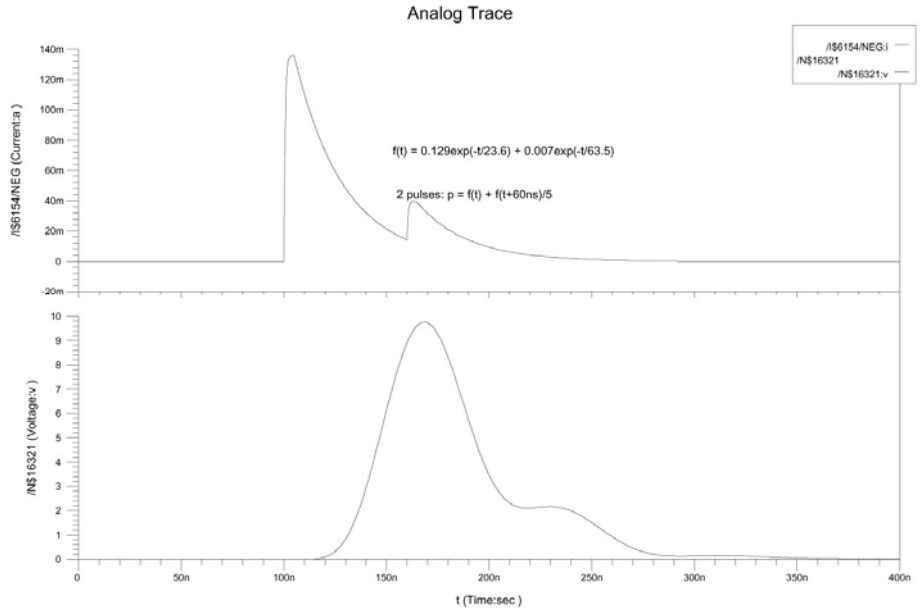

Figure 9. Two pulses - the additional pulse is 60ns after the full pulse.

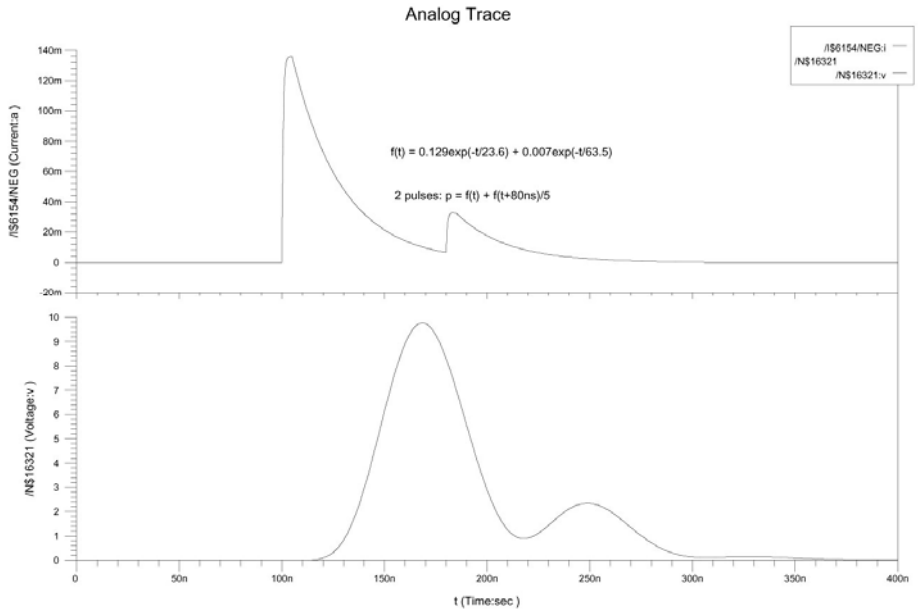

Figure 10. two pulses - the additional pulse is 80ns after the full pulse.