KOTO ADC Boards – 1.2V Power Caps

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Problem:

Compressed Data transmission between the ADC Boards and L2 showed Rx errors occurring in the L2 boards, in sync with the L1 Accept pulses.

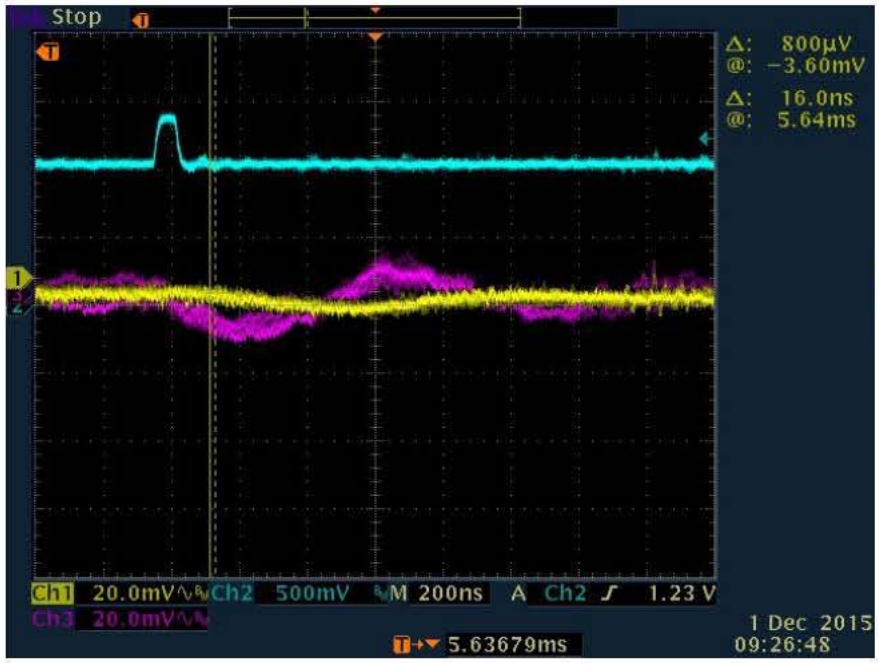
The errors were traced back to the ADC Modules, i.e. to temporary (~ 500ns) Voltage drops in the VCCINT=1.2V. These Voltage drops were caused by a temporary increase of current demand from ~1.4A to ~2.3A, due to intense activity inside the FPGA during compression.

Solutions:

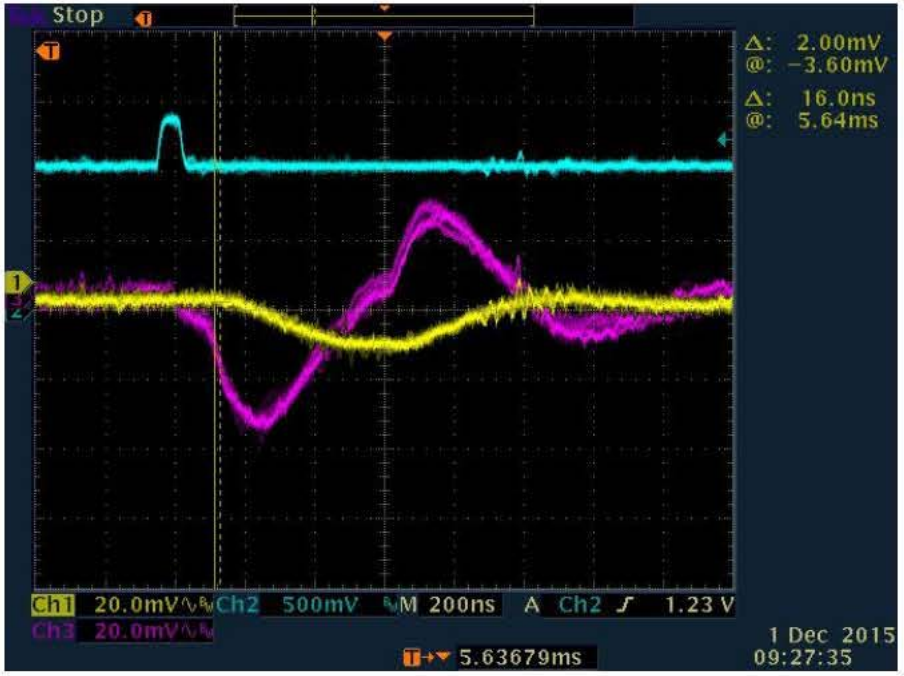
- **Modify firmware to reduce temporary current demand;**
- **Install more capacitors and improve current path;**
- **Combination of the two above.**

Voltage Test with Compression OFF/ON 2071.sof

H2 **Compression OFF** OK



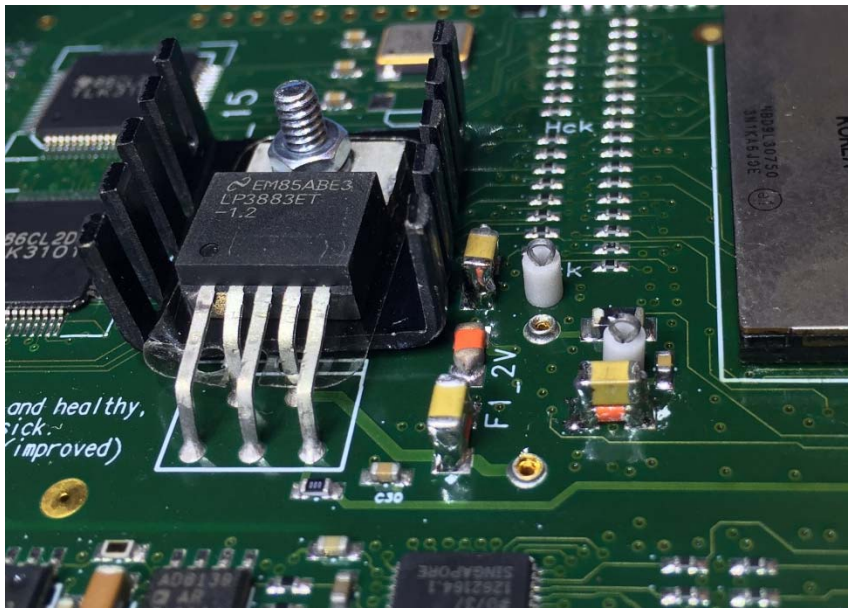
Compression ON Bad

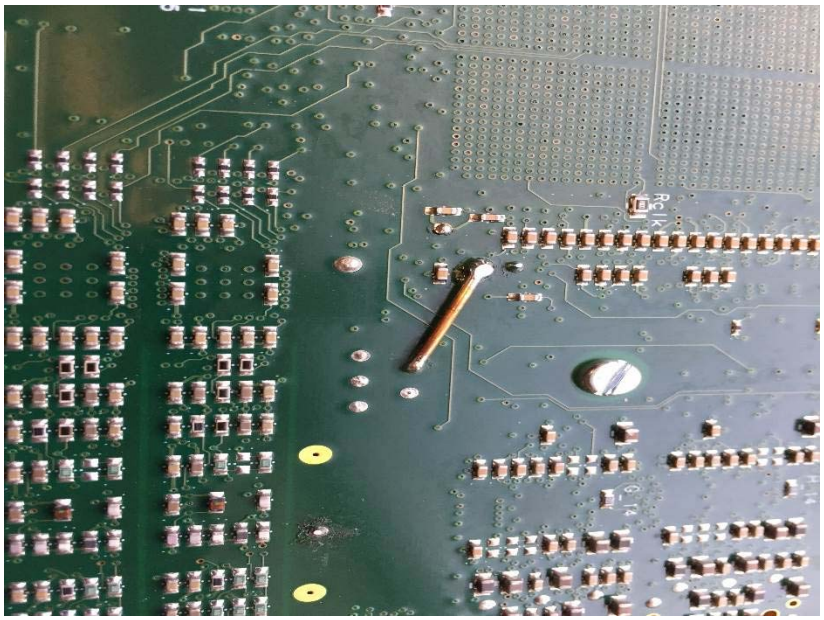


Channel 2 =L1A pulse
Channel 3 = VCCINT = 1.2Vcc
Channel 1 = +1.2V_PLL = 1.2Vcc filtered

The voltage drops with compression OFF are causing no noticeable problems in FPGA functionality.

Hardware Solution





The added caps are the 3 yellow ones in the picture.
Their sizes are 1206; part # GRM31CR60G227ME11L

On Top Side:
Install three 220uF ceramic caps over C26, C27, C29.

On Back Side:
Install wire jumper as shown.

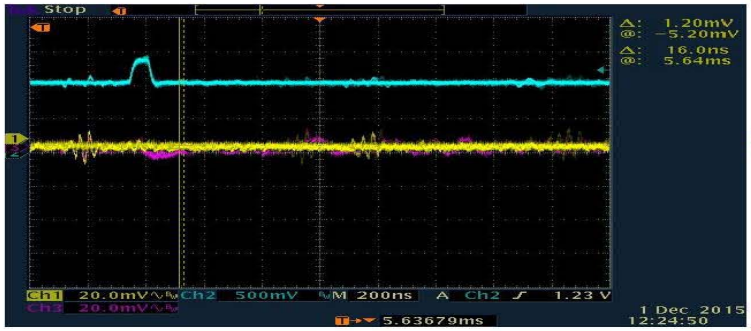
Several ways to reduce the power glitches were studies and tried; here in the best solution.

Voltage Test with Compression OFF/ON (with three 220uF caps installed)

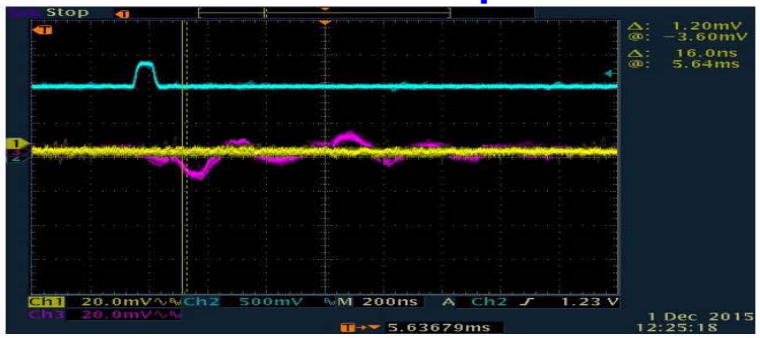
H2 with three 220 capacitors

v2071

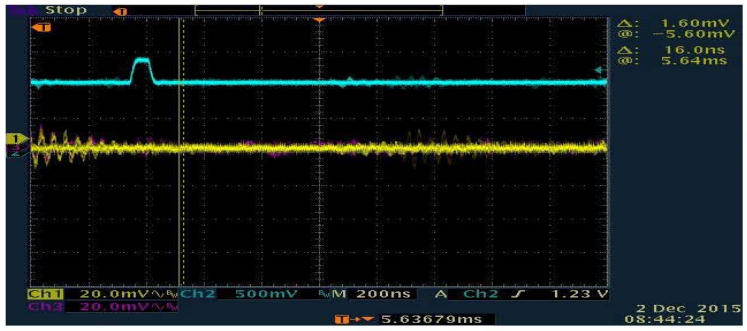
Compression OFF

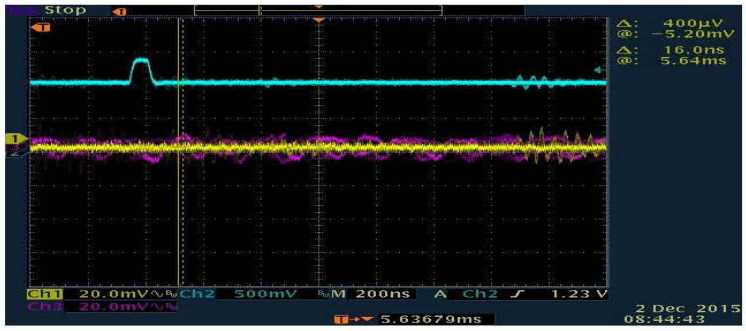


Compression ON



v2098





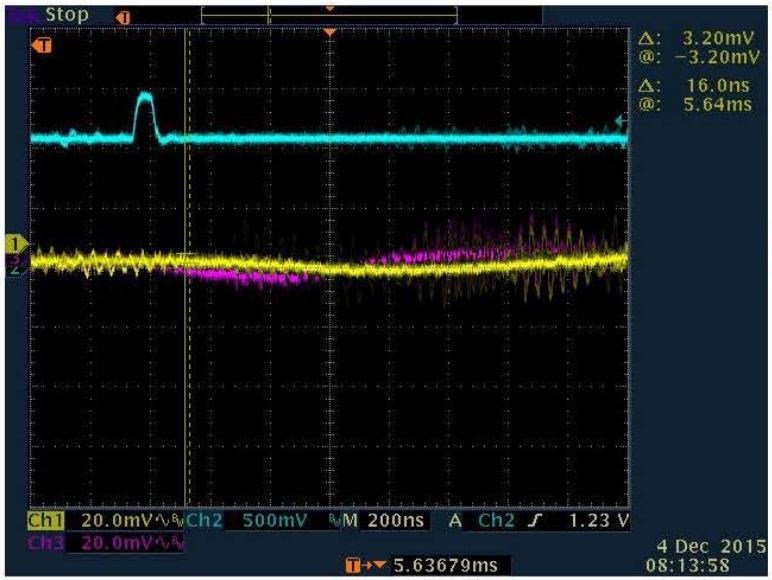
Channel 2 =L1A pulse
Channel 3 = VCCINT = 1.2Vcc
Channel 1 = +1.2V_PLL = 1.2Vcc filtered

After installing the 3 caps, the voltage drop with compression ON is smaller that when compression was OFF with no caps.

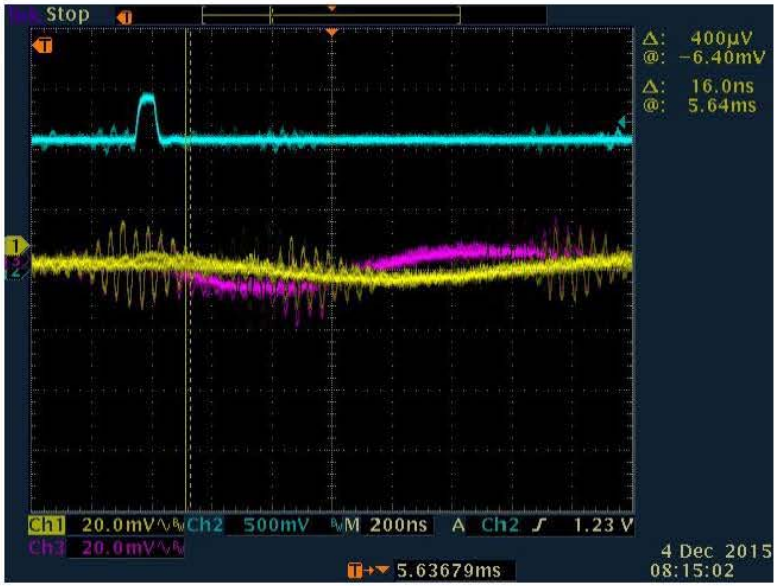
500MHz Board Voltage Test with Compression OFF/ON (No Caps)

Before Modification
#30

Compression OFF



Compression ON

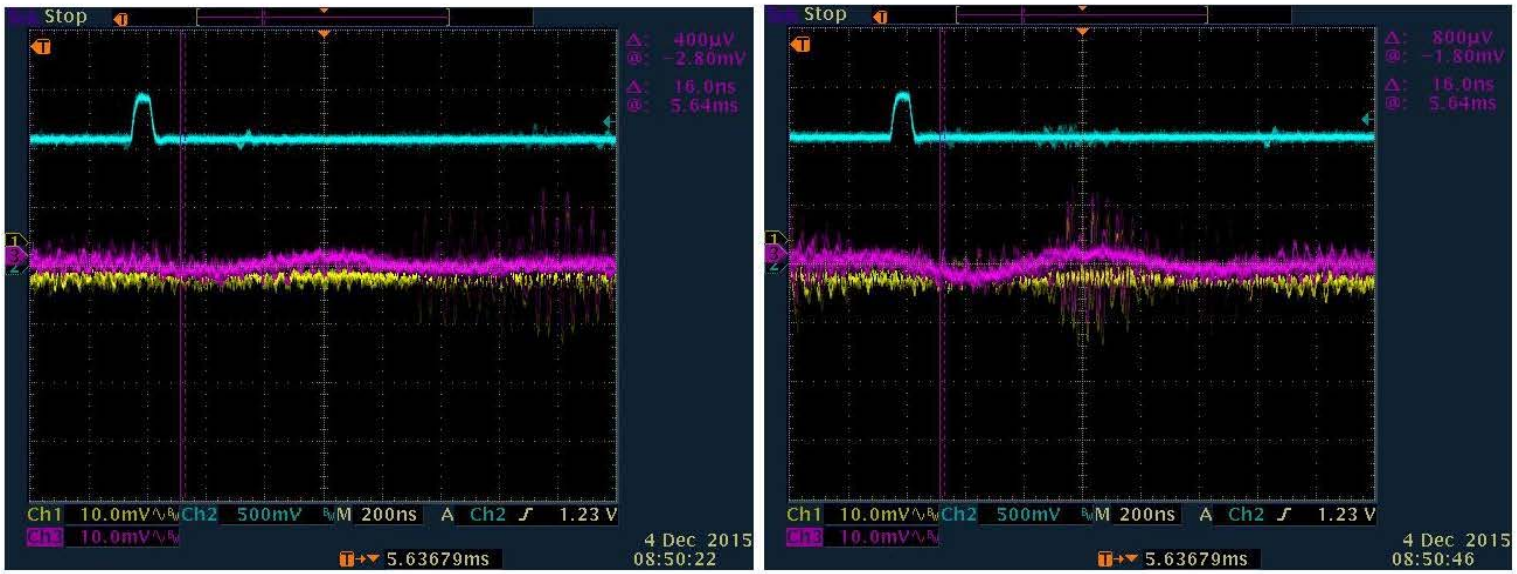


Channel 2 =L1A pulse
Channel 3 = VCCINT = 1.2Vcc
Channel 1 = +1.2V_PLL = 1.2Vcc filtered
No real problem shown on the 500Mhz board.

500MHz Board Voltage Test with Compression OFF/ON (With two 100uF Caps)

Compression OFF **Compression ON**

After Modification #30



Channel 2 =L1A pulse
Channel 3 = VCCINT = 1.2Vcc
Channel 1 = +1.2V_PLL = 1.2Vcc filtered
No real problem shown on the 500Mhz board.

Conclusions

This solution was tested on 8 modules of 125MHz ADC and 6 modules of 500MHz ADC, and the results are very similar.

This solution will improve power supply behavior with different firmware versions.

It is very important that every new firmware version is tested for power consumption. Excessive power demand may cause supply failure, which may damage the FPGA.