Custom 12-Bit, 500MHZ ADC/Data Processing Module for the KOTO Experiment at J-Parc

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***Abstract*—The paper presents a custom 4-Channel, 12-Bit, 500 MHz ADC/Data Processing Module, designed for the Step1 of the KOTO Experiment at J-Parc, Japan. This 6U VME Board will receive signals from the Beam Hole Photon Veto Detector, and will be one of the several different ADC Modules in the Experiment's Data Acquisition System (DAQ). In KOTO, the main ADC/DAQ system runs at a 125 MHz simultaneous sampling rate, provided by one low jitter 125 MHz system clock. The 500 MHz ADC Module receives this system clock and multiplies its frequency by four with a local Zero Delay Clock Generator. The four analog input pulses are amplified and passed to the 12-Bit, 500MHz monolithic pipeline ADC chips. After sampling, data are processed locally with a field programmable gate array (FPGA). The module is provided with a pipeline, up to 40us (20,480 samples) long, which stores the acquisitions, awaiting the system Level 1 trigger pulse. After a trigger, data are packed and buffered for readout. The readout can be performed via the VME32/64 backplane, or via the two front panel optical links. Designed specifically for the KOTO Experiment, this module can also be used in many other Physics applications. The board can receive the analog input signals in both single ended or differential modes and it can run with a local oscillator or with input clocks in the range of 32.5MHz to 550MHz. The design and preliminary test results will be described.**

Keywords-ADC; DAQ; trigger.

I. INTRODUCTION

We present a custom ADC/DAQ Module designed for the Step-1 phase of K0TO [1], a high energy physics Kaon experiment at the Japan Particle Accelerator Research Complex (J-PARC). The purpose of KOTO is to measure the rate of the rare decay $KL \rightarrow \pi^0 \nu\nu$, predicted by the Standard Model to happen only once every 3.3×10^{11} KL decays. The Experiment plans to shed light on the mechanism responsible for CP in the quark sector.

This 4-Channel, 500MSPS ADC Board will receive analog signals from the Beam Hole Photon Veto Detector, and will be one of the many custom modules in the KOTO DAQ System.

II. ARCHITECTURE

The Block Diagram of the ADC module is presented in Figure 1. We can identify three main blocks: the signal conditioning and conversion block, the data processing block, and the interface block.

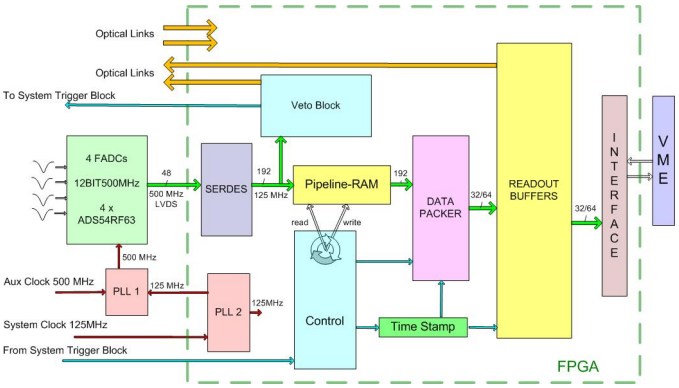

Figure 1. Block Diagram of the 500MHz ADC Module.

A. Signal Conditioning and Conversion Block

Figure 1 presents the Schematic of one ADC channel, configured to run at 500MSPS and with an input signal excursion between 0 and -2V. The input channel bandwidth is about 105MHz at -3dB. In this configuration, the analog signal is amplified, offset, and applied to the A/D chip ADS54RF63, by TI.

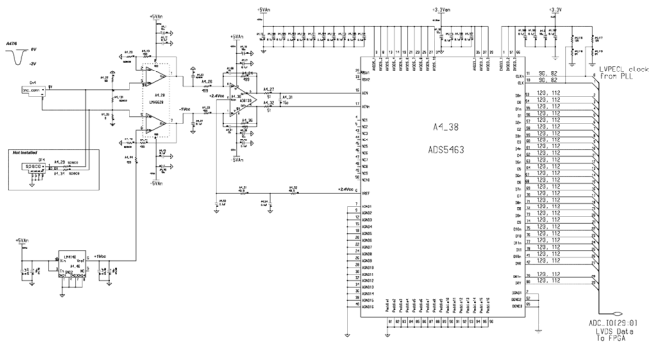

Figure 2. Schematic of one 12-BIT, 500MSPS ADC Channel.

Signal gain, offset, and bandwidth can be adjusted by changing a few passive components. On the same PCB, any channel can be independently configured for a differential or for a single-ended input signal. The implementation shown is single-ended, using BNC connectors. The differential configuration uses LEMO connectors (DF4 in Figure 2).

In the KOTO Experiment, this module will work on the low jitter, 125MHz system clock. This clock is applied to a Zero Delay PLL Clock Generator ICS8735-21, which provides the 500MHz sampling clocks for the ADC chips. The module can also work with a different input clock, in the 31MHz to 700MHz range, as well as with a locally generated clock.

B. Data Processing Block

All four channels are serviced by one single Field Programmable Gate Array (FPGA), Altera EP2S60F1020C5 chip from the STRATIX II family [2]. The 500 MHz digitized samples are passed directly to the FPGA, were the data stream is first deserialized and reduced in frequency by a factor of four. All subsequent data processing steps take place at the 125MHz system clock frequency.

Beam Hole Photon Veto related values are calculated in real time and sent to the System Trigger block via a front panel Optical Link.

Each ADC module is provided with a pipeline, up to 40us (20,480 samples) long, which stores the acquisitions while awaiting the system trigger pulse. After a trigger, data are packed and buffered for readout. Depending on the volume of data, readout can be performed via one of the two front panel Optical Links, or via the VME64x backplane.

C. Interface Block

System interfacing can be done in both LVDS and LVTTL standards, using an RJ45 connector and several right angle headers, all placed on the front panel. The functionality of the I/Os is configurable.

The module is also provided with two Optical Link transceivers with up to 3.125Gbps each. The links lead to the local FPGA, so their functionalities are configurable to serve different purposes, depending on the application. For KOTO, one optical output is designed for the Beam Hole Photon Veto, and the second one, for data read-out.

III. CONCLUSIONS

Two prototypes 4-channel, 500MSPS, 12-Bit ADC Modules were built so far. They were successfully tested in Chicago, as well as at the April 2010 JPARC-KOTO Beam Test, in Sendai, Japan.

Figure 3 presents one of the ADC modules, that was assembled with a single ended configuration for all channels. Preliminary test results show an input noise of about 1.3 LSB for a sampling rate of 500MHz, and with a one-pole input filter at about 110MHz.

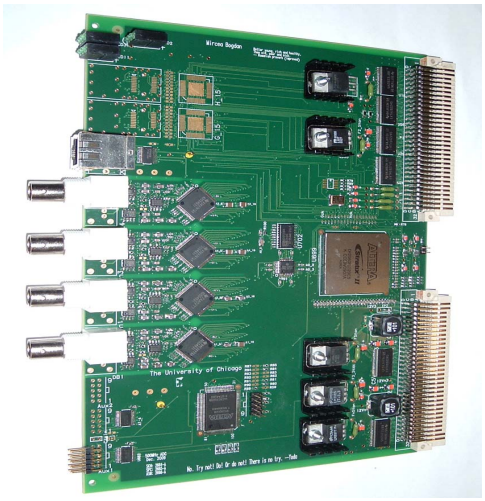

Figure 3. Prototype 4-Channel 500MSPS ADC/DAQ Module. This PCB was assembled for single ended input configuration on all channels. The two front panel Optical Link transceivers were not installed. Data readout is performed via the VME backplane.

Figure 4 presents a VME recording of PMT pulses, digitized by the 500MSPS ADC Module. For this recording, an original CsI/PMT pulse was normalized and reused as input with an Arbitrary Waveform Generator.

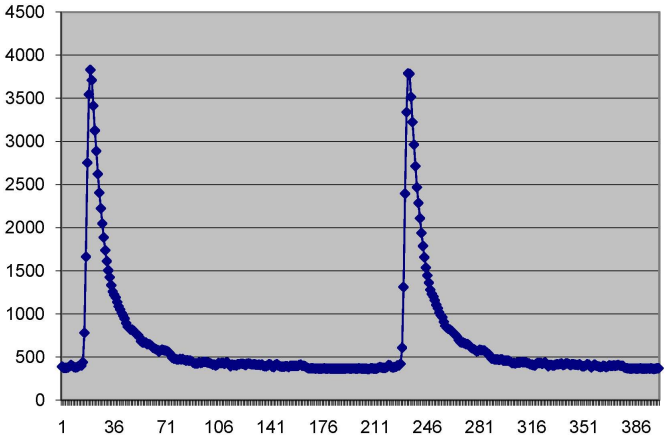

Figure 4. VME recording of PMT pulses, digitized by the 500MSPS ADC Module.

This ADC module was designed to be used in the KOTO DAQ System, but it can also offer a great level of configurability. With minor firmware changes, and/or passive component modifications, this module can easily be integrated in many other systems, and for many other applications.

REFERENCES

[1] E14: Proposal for $K^0_L \rightarrow \pi^0 \nu\nu$ Experiment at JParc, approved July 2007.

[2] Altera Corporation, Stratix II Device Handbook, v.4.5., July 2008.