KOTO-style signal

LVPECL clock from PLL

A4_38

ADS5463

ADC_IO[29:0]
LVDS Data
To FPGA

Notes:
This ADC channel can be implemented in differential or in sigle ended configurations.
The components marked "space" are not to be installed.

Engineer	M.Bogdan			
Drawn by	M.Bogdan			
R&D CHK		TITLE		Size C
DATE:	10/22/10	**12BIT, 500MHz ADC**		
TIME:	11:00 am	4 Identical Channels on Board		
QA CHK		REV B	DRW. 2664	Sheet 2_j of 12