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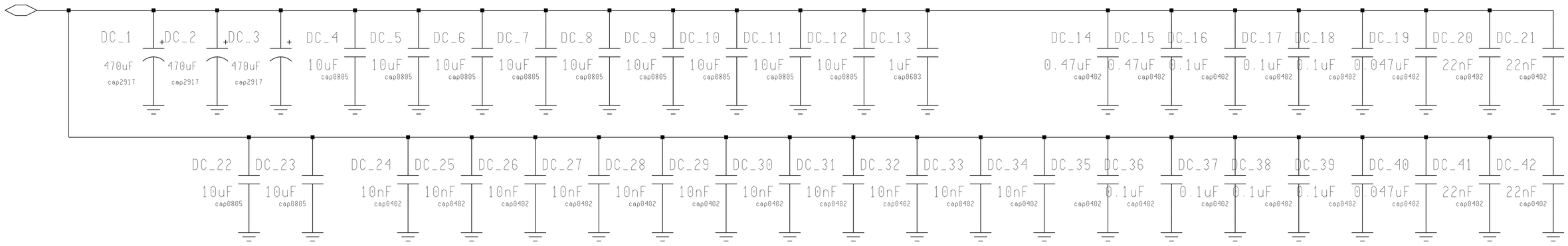

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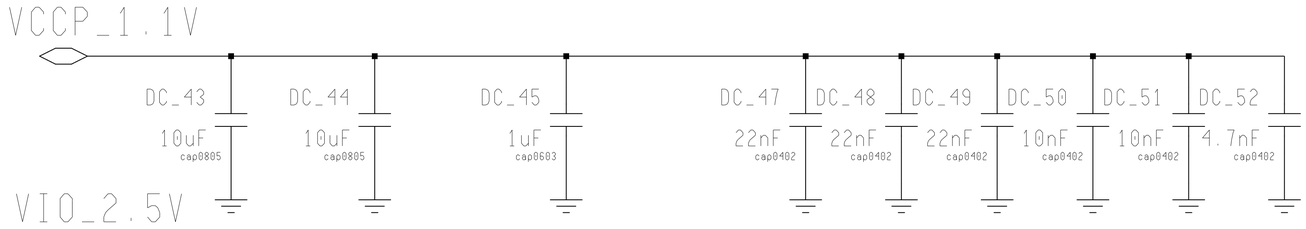
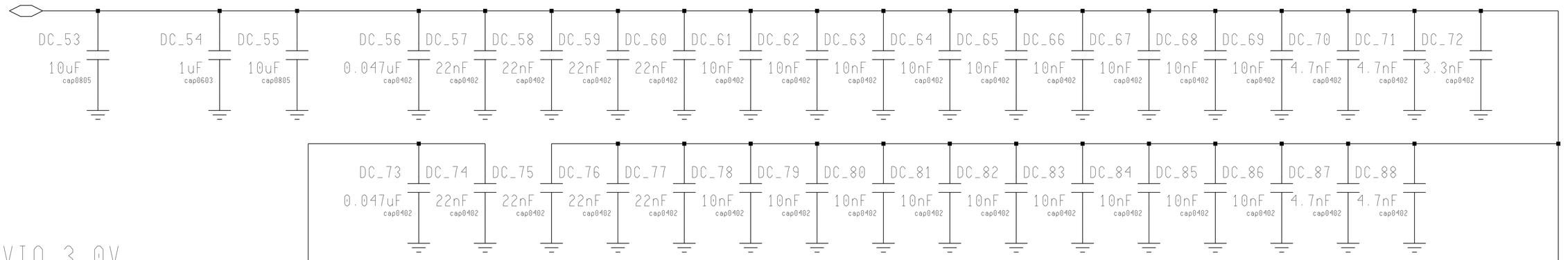


VIO_2.5V



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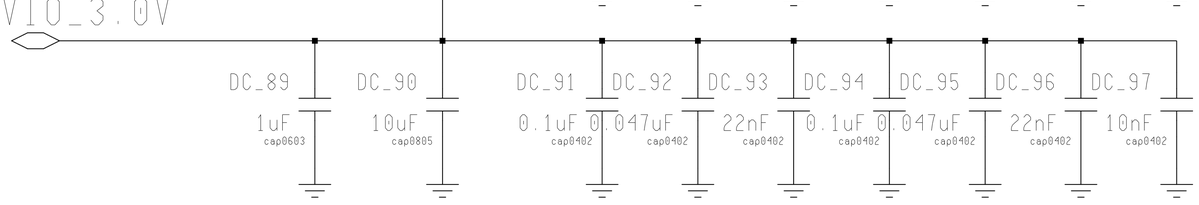

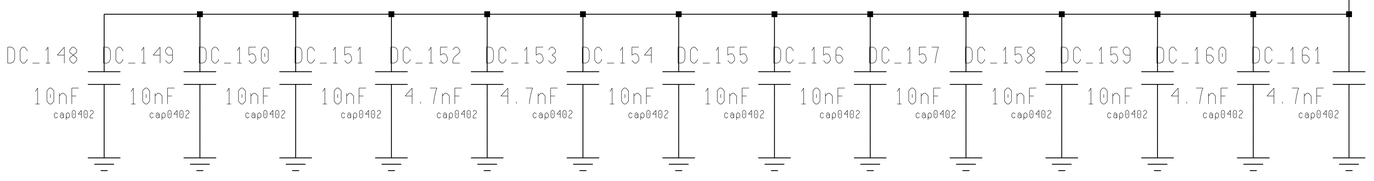

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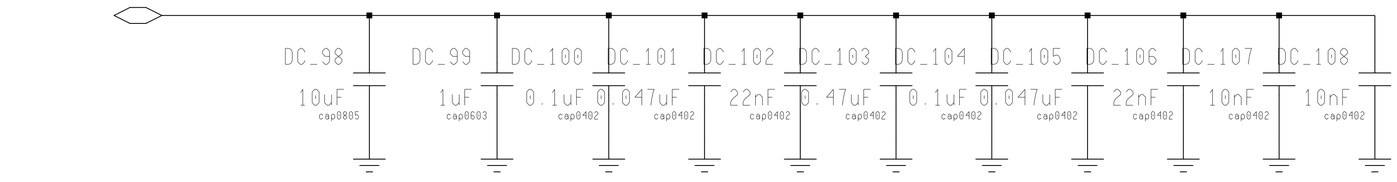

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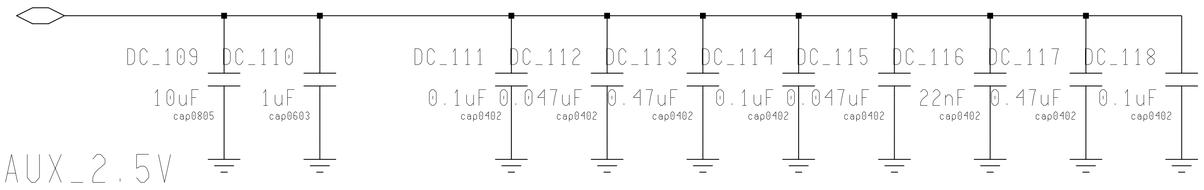

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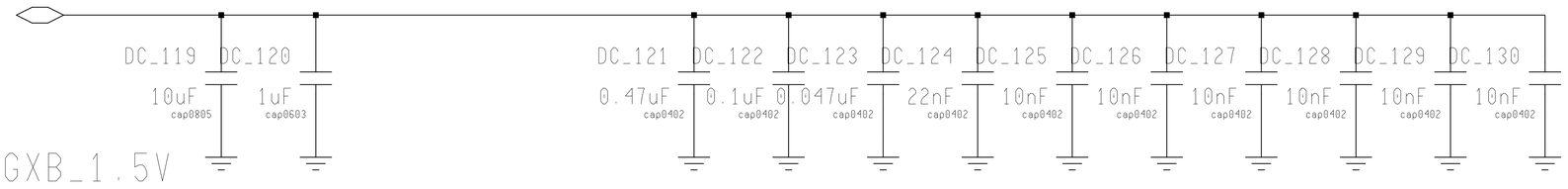

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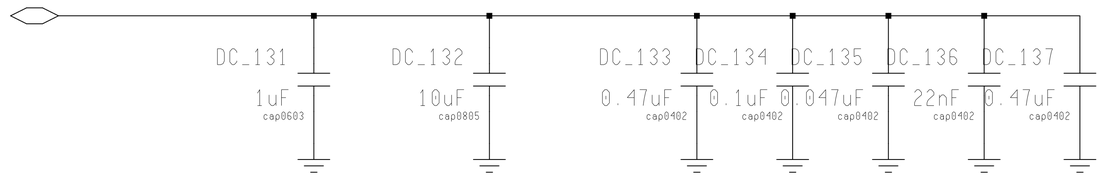

Engineer: M. Bogdan	*DAMIC - ODILE Module*		
Drawn by: M. Bogdan	**FPGA Decoupling Circuit**		
DATE: 2/7/2019	**The University of Chicago**		
SPC#2938 ASM#2939	REV. A	DRW. 2937	Sheet 7