

1

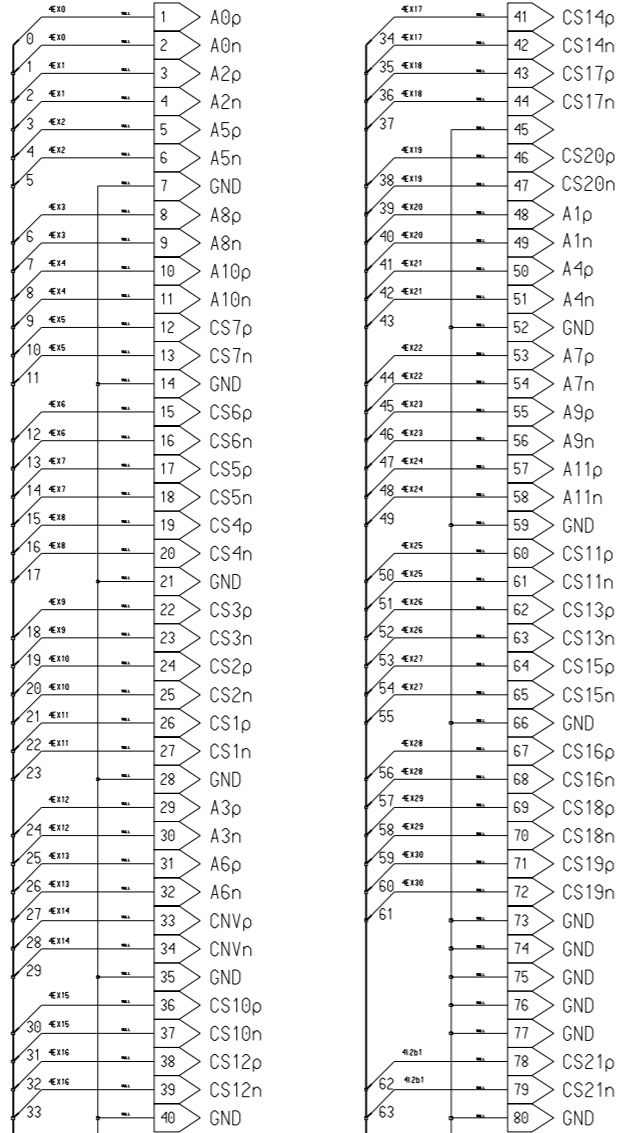
2

3

4

FP4: LVDS Input

Note: FP4 is a 80-pin Honda connector

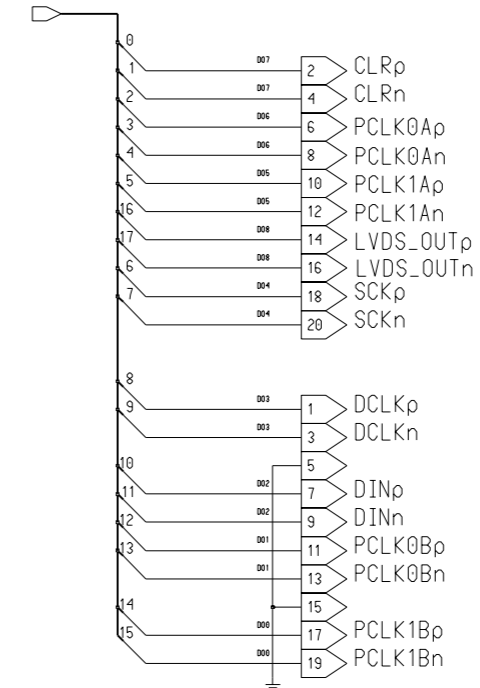


DigOut1(63:0)

FP3 LVDS I/O

Note: FP3 is a 20-pin connector

DigOut2(17:0)



Engineer	M. Bogdan	The University of Chicago 5640 S. Ellis Ave. Chicago, IL 60637		
Drawn by	M. Bogdan			
R&D CHK		LVDS_I/O Connectors QEBB - LVDS I/O - SAB		
DATE:	1/09/05			
TIME:	1:30 pm			
QA CHK		REV A	DRW. B-2572	Sheet 2 of 2

1

2

3

4