

TFM – Status Report

Preliminary Testing of Power Supplies

3/25/2020

Mircea Bogdan

TFM – Status Report

Preliminary Testing of Power Supplies:

- Simple Manual Power Supply Control
- Test of each supply individually:
 - Static Loads Only
 - Transition Times
 - Individual Supply Efficiency: $V_{out} * I_{out} / [12V * (I_{12V_2} - I_{12V_1})]$
- Test of all Supplies Together
- No Power Sequencing

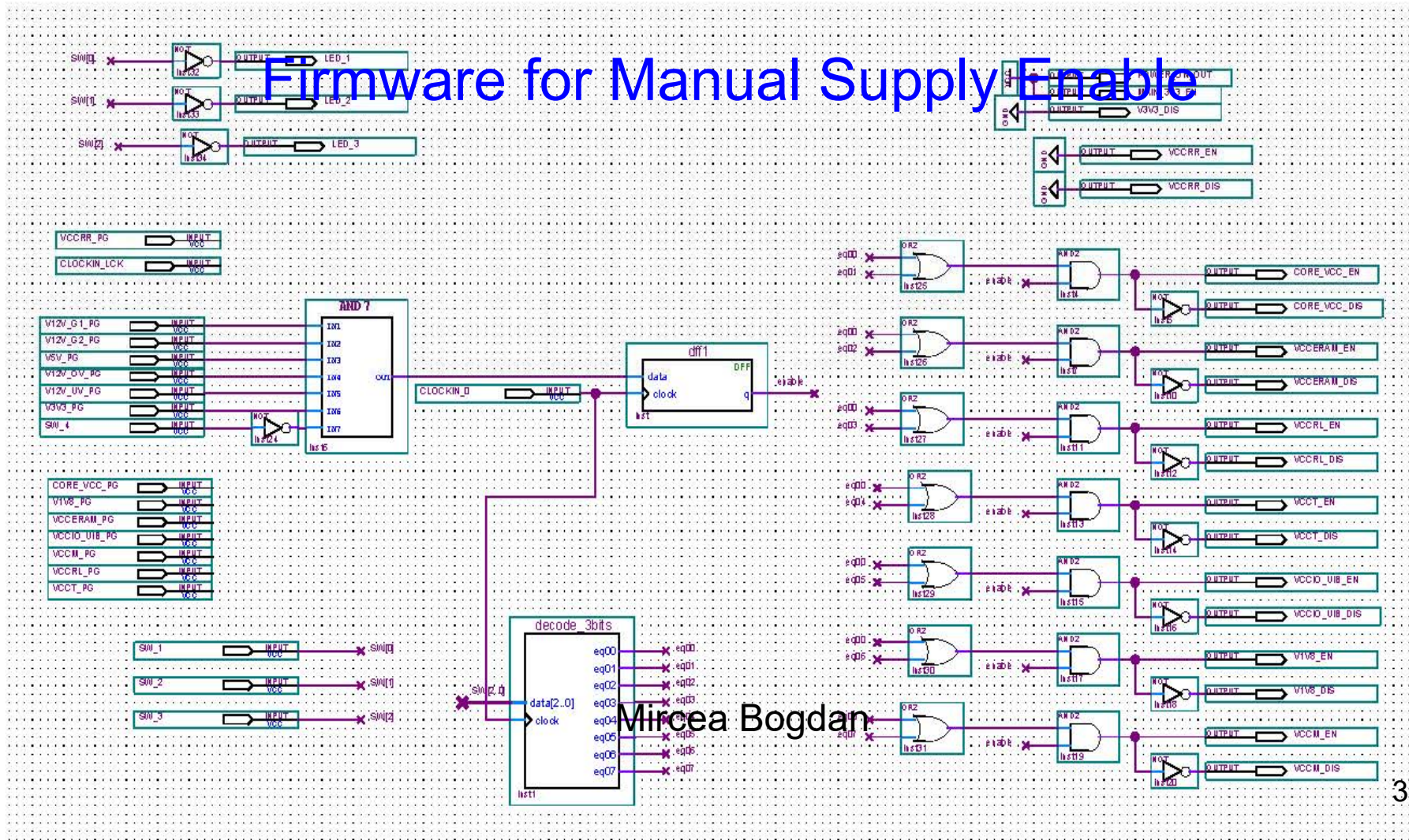
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Testing Firmware - 1

Date: March 12, 2020

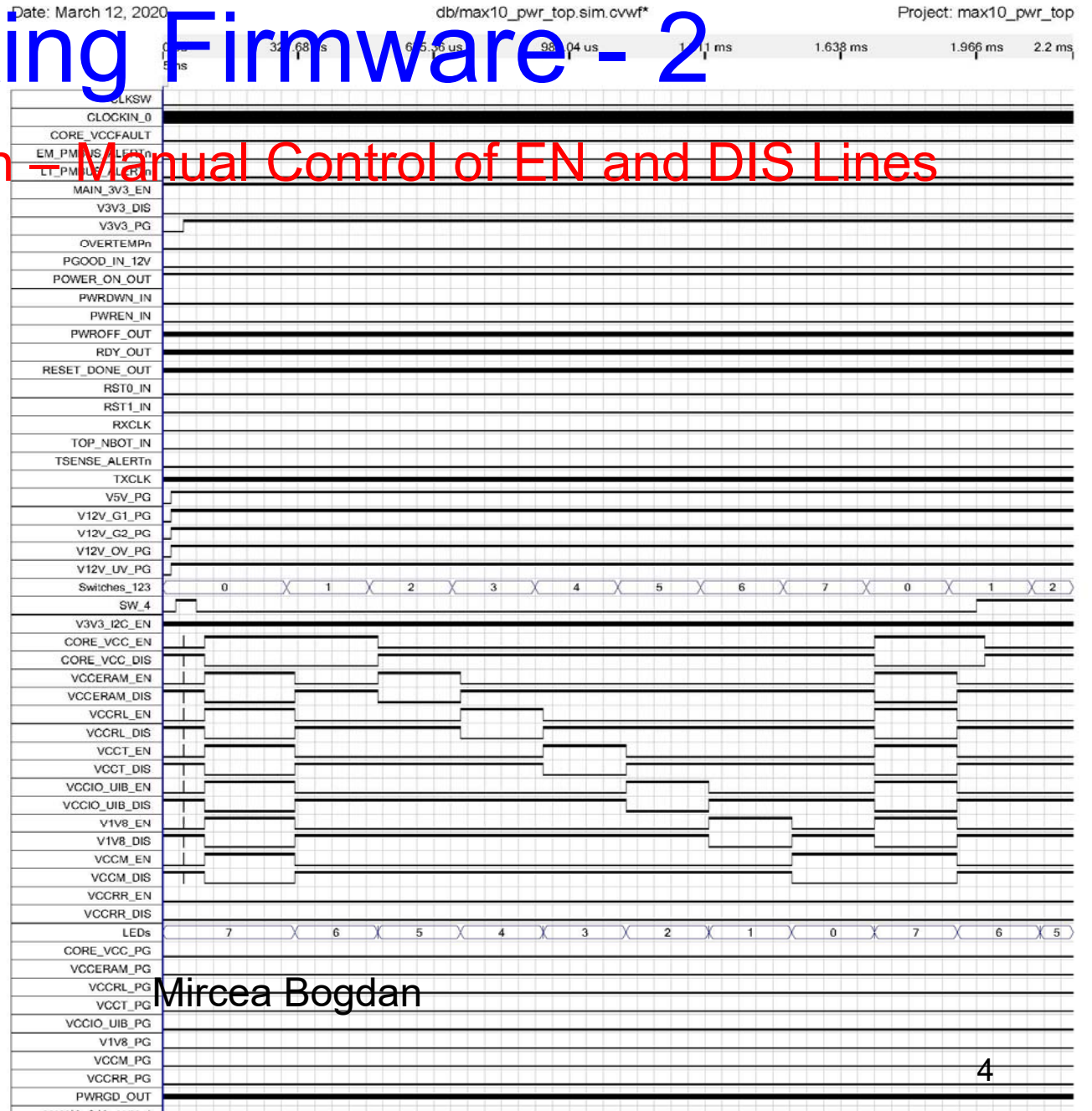
max10_Logic.bdf

Project: max10_pwr_top



Testing Firmware - 2

Firmware Simulation - Manual Control of EN and DIS Lines



Testing Firmware - 3

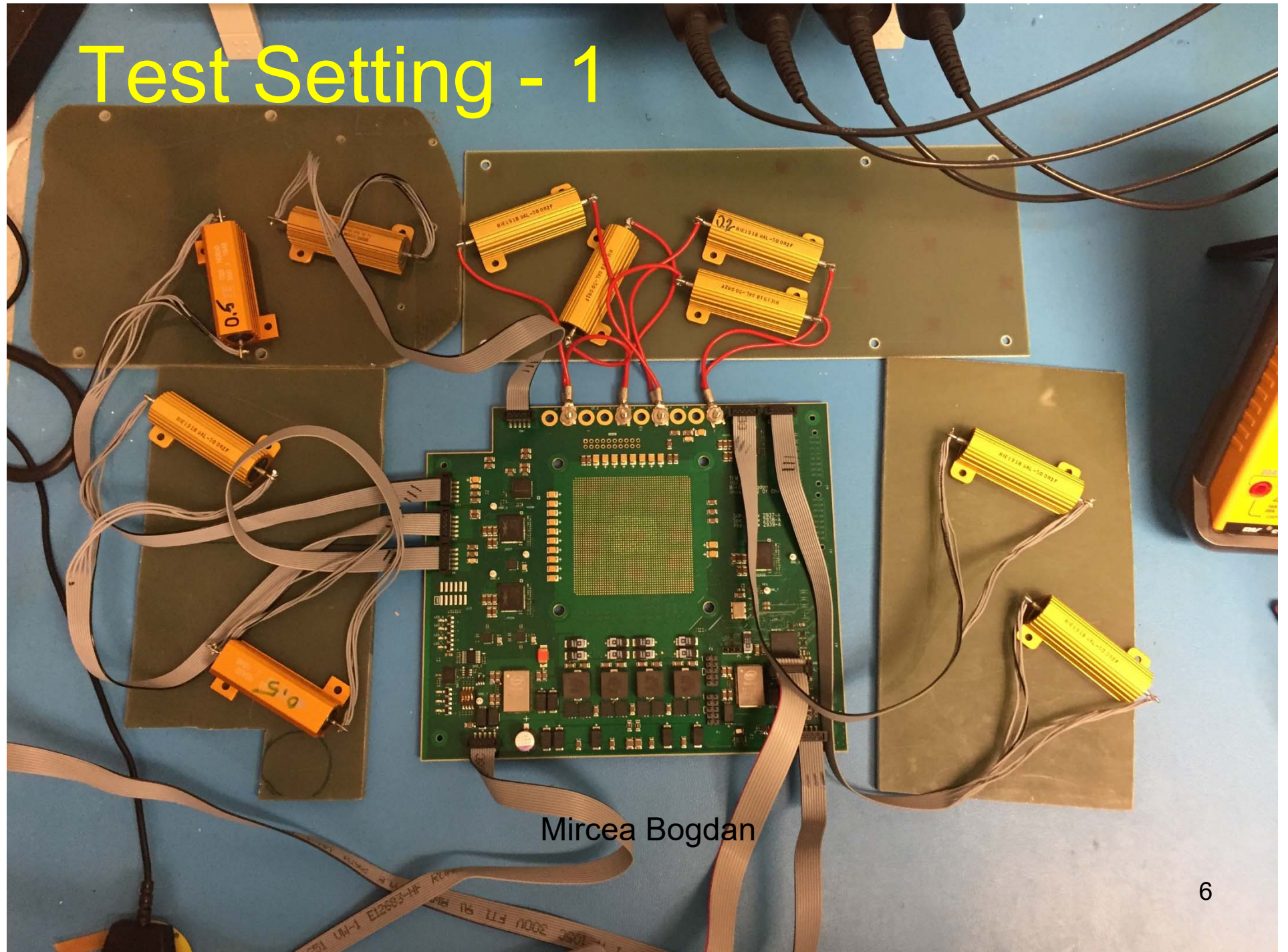
MAX10 Signal Tap – Manual Control of EN and DIS Lines

The image displays two screenshots of the Signal Tap Logic Analyzer interface. Both screenshots show the 'Instance Manager' with 'auto_signaltap_0' in a 'Waiting for trig...' state. The top screenshot shows a waveform for 'log: Trig @ 2020/03/15 10:44:35 (0:3:40.0 elapsed)'. The bottom screenshot shows a waveform for 'log: Trig @ 2020/03/15 10:30:14 (0:0:13.3 elapsed)'. Both waveforms show signals for 'VCCRL_EN' and 'VCCRL_PG' with a time axis from -8192 to 57344. A red text overlay in the bottom screenshot reads 'Power OK after ~ 1ms of Power Enable'. The bottom screenshot also includes a 'Hierarchy Display' on the left and a 'Data Log' on the right.

Power OK after ~ 1ms of Power Enable

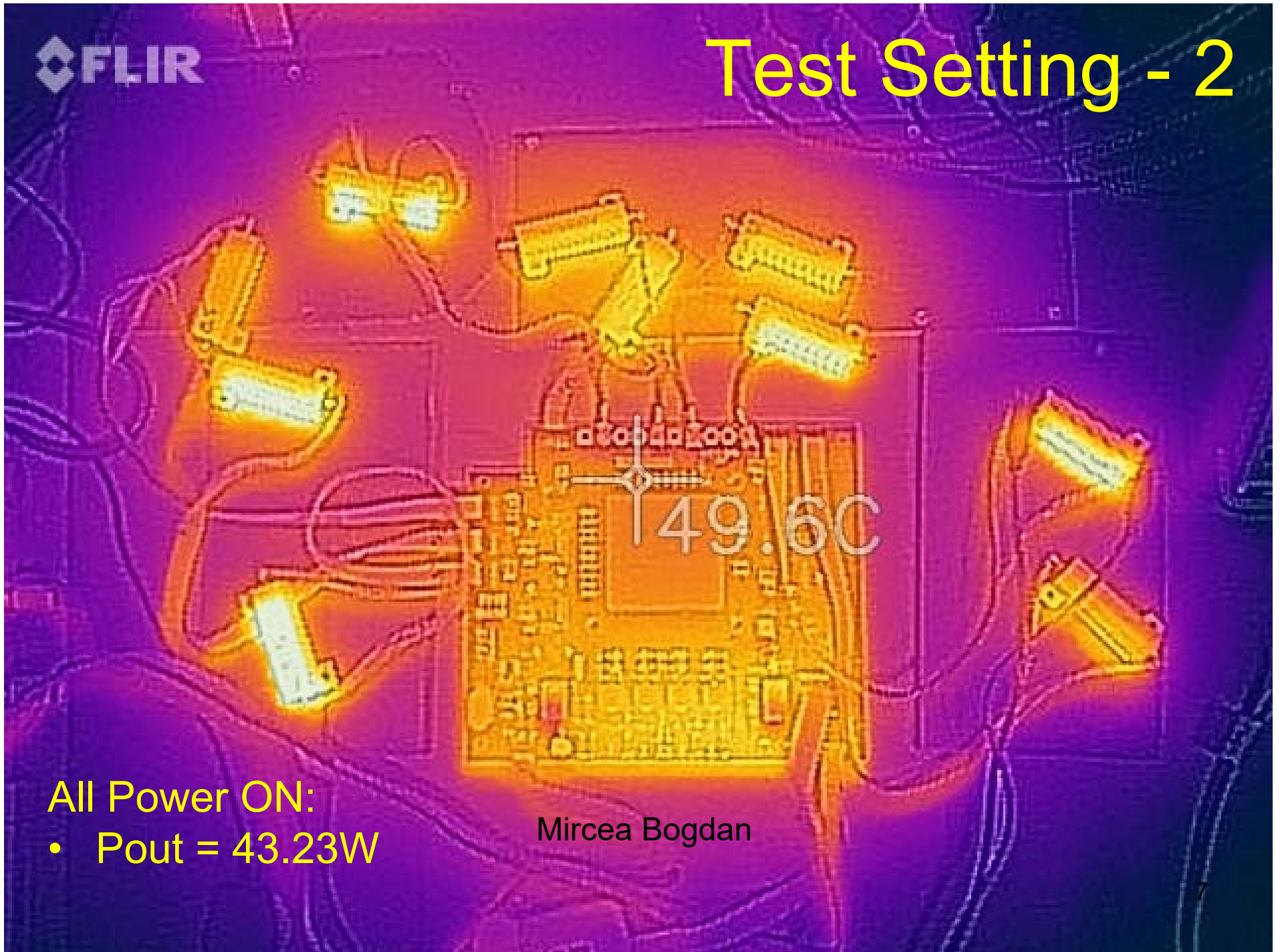
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Test Setting - 1



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Test Setting - 2



All Power ON:

- $P_{out} = 43.23W$

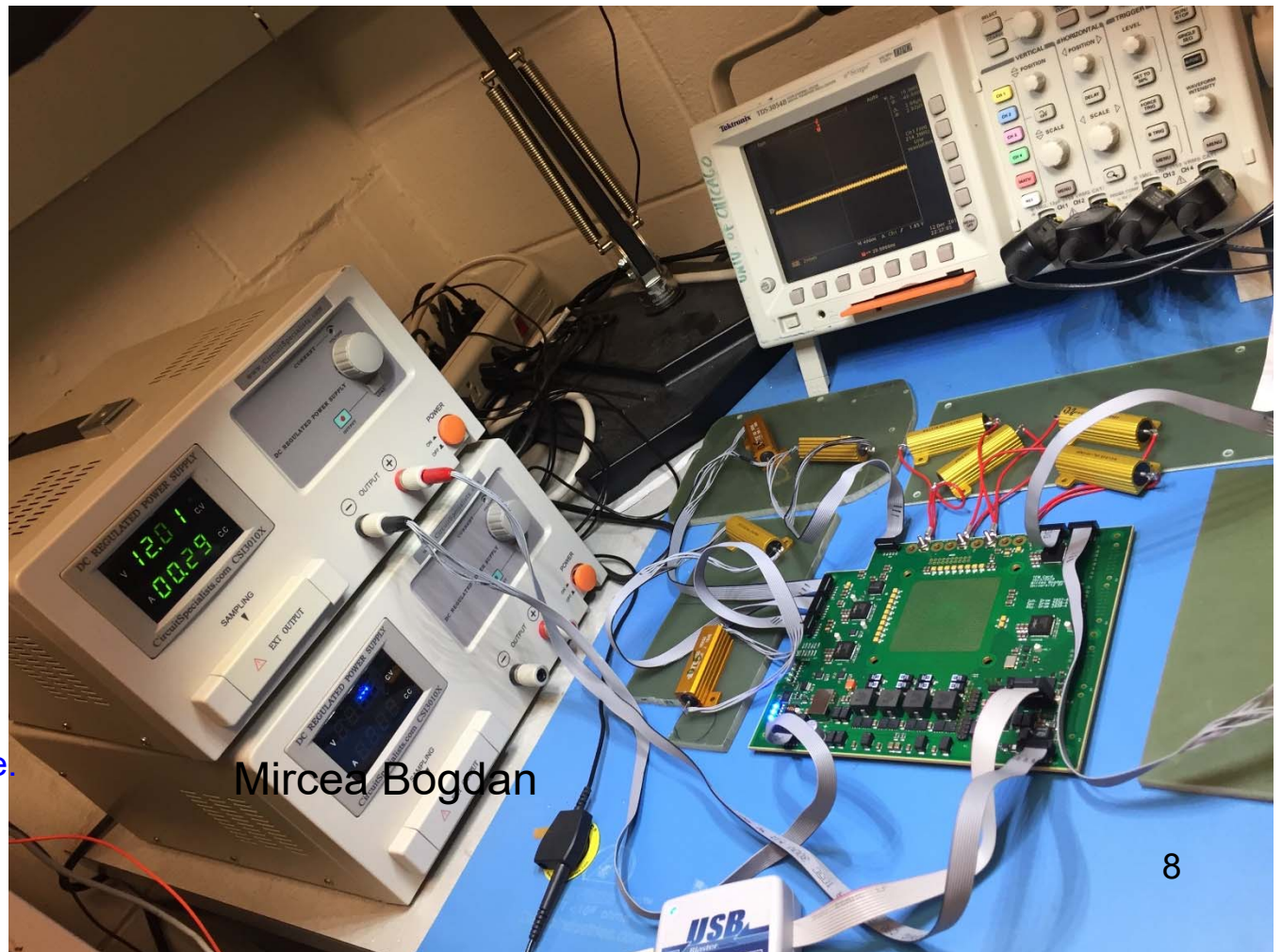
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Test Setting - 3

Power ON:

- 5V_STBY
- 3.3V_STBY
- 3.3V_Main
- 12V_2
- 12V_2
- MAX10 sof ON

This is not the future IDLE state.

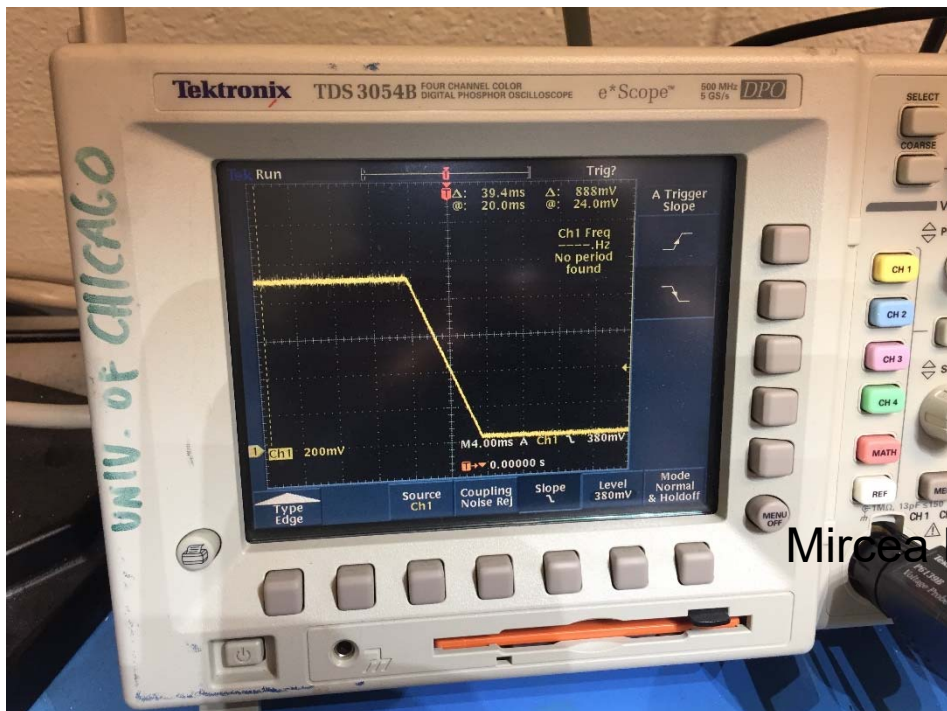
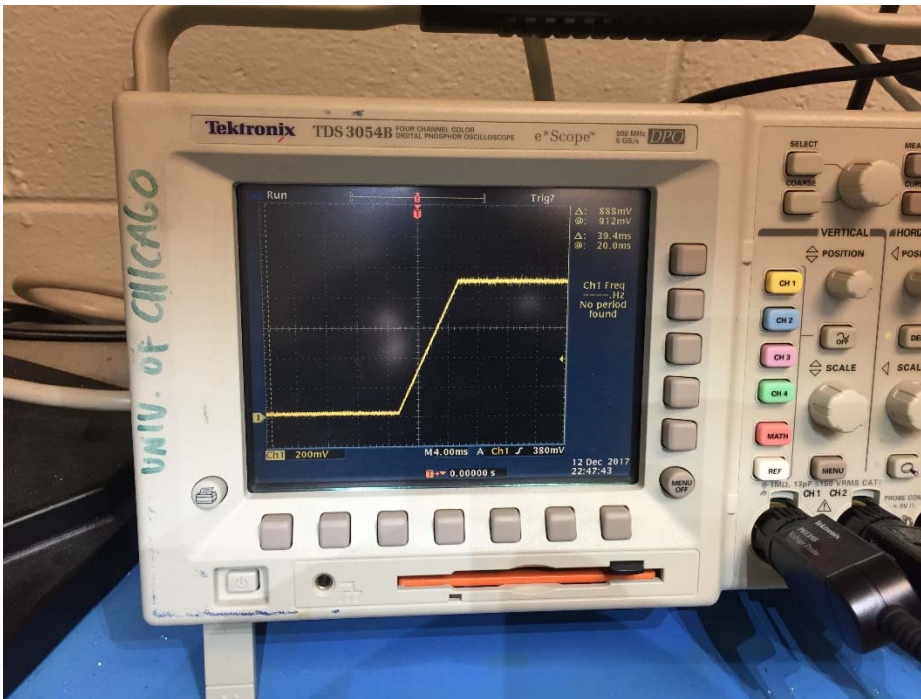


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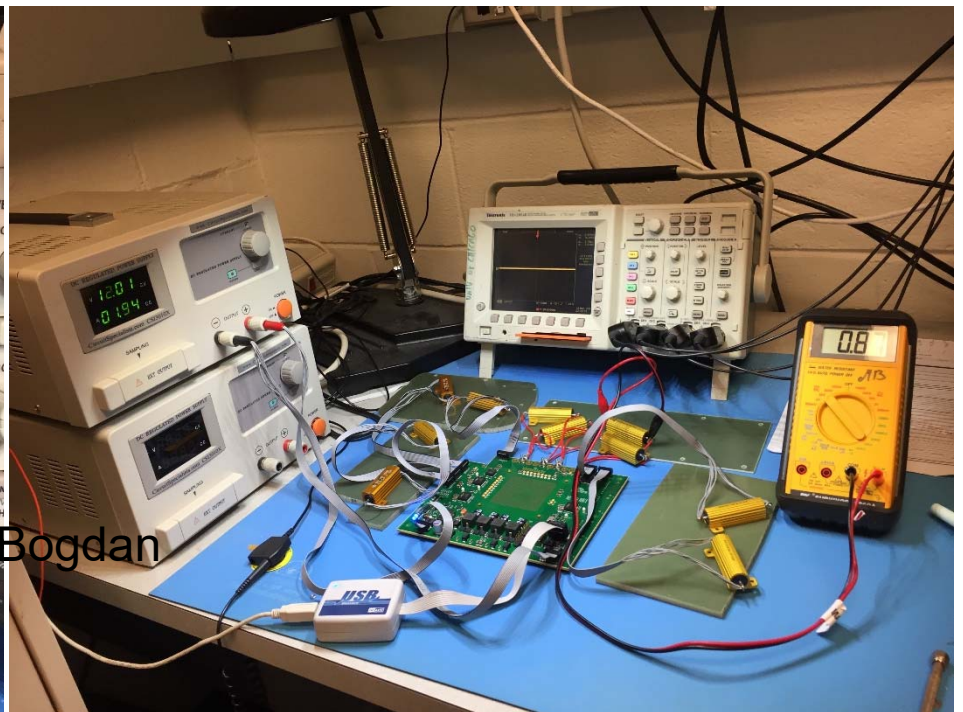
TFM - Core VCC

- $V_{out} = 0.9V$
- $I_{out} = 17.4A$
- $T_r \sim 8ms$
- $T_f \sim 8ms$

LTC3884



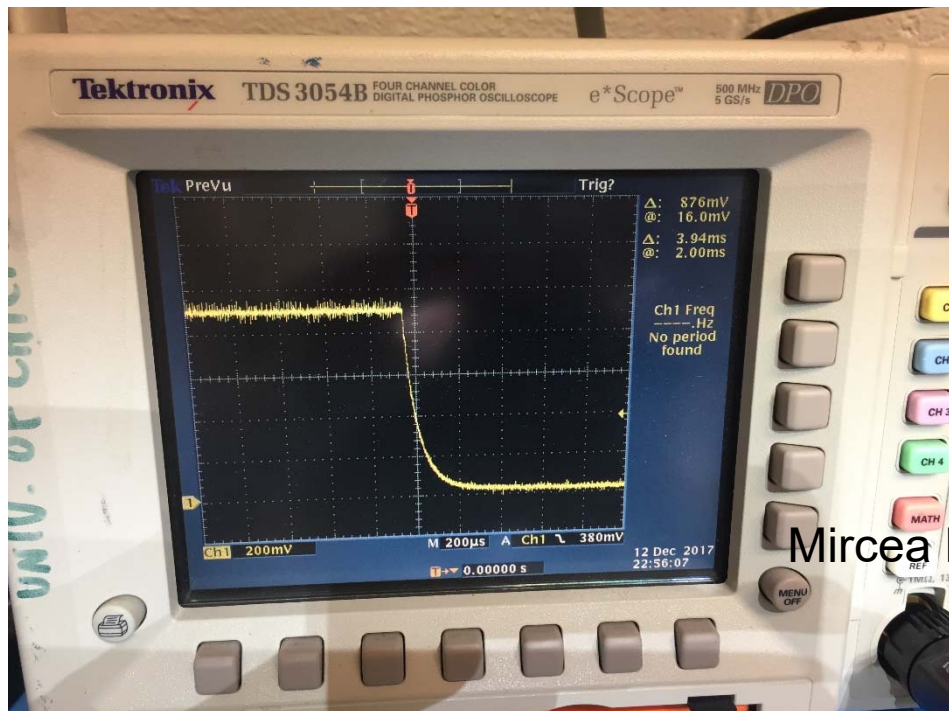
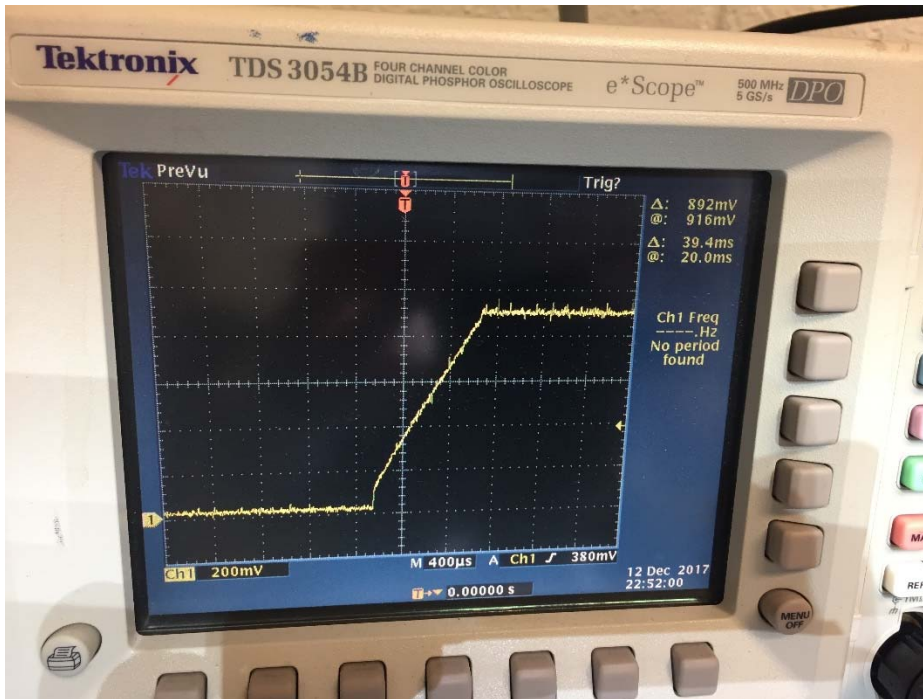
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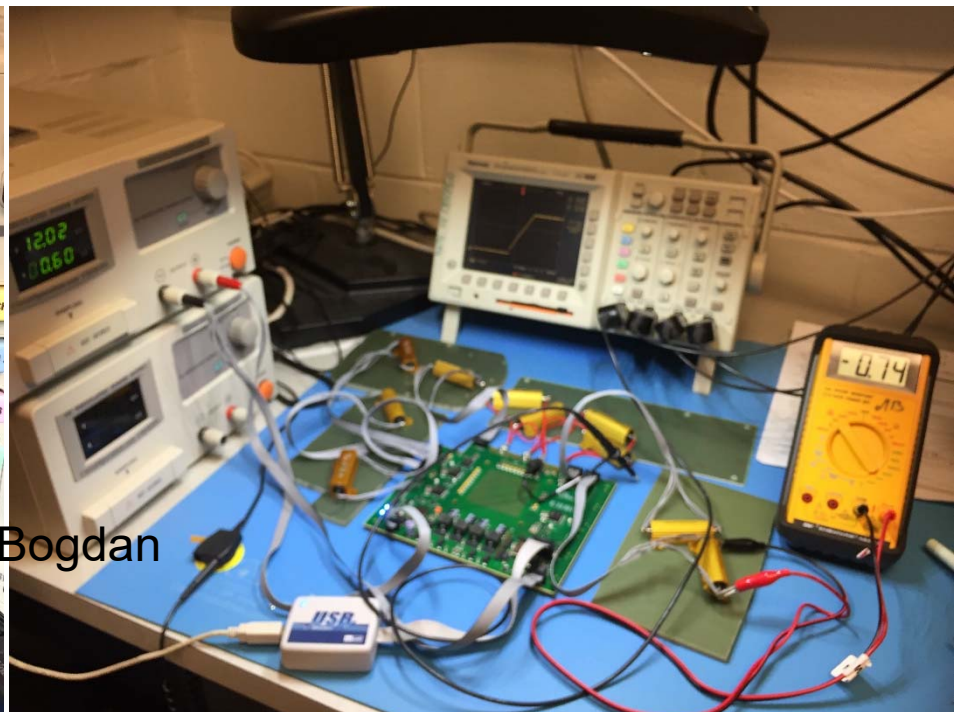
TFM - VCCERAM

- $V_{out} = 0.9V$
- $I_{out} = 3.7A$
- Efficiency = 87%
- $T_r \sim 800 \mu s$
- $T_f \sim 250 \mu s$

EN63A0QI

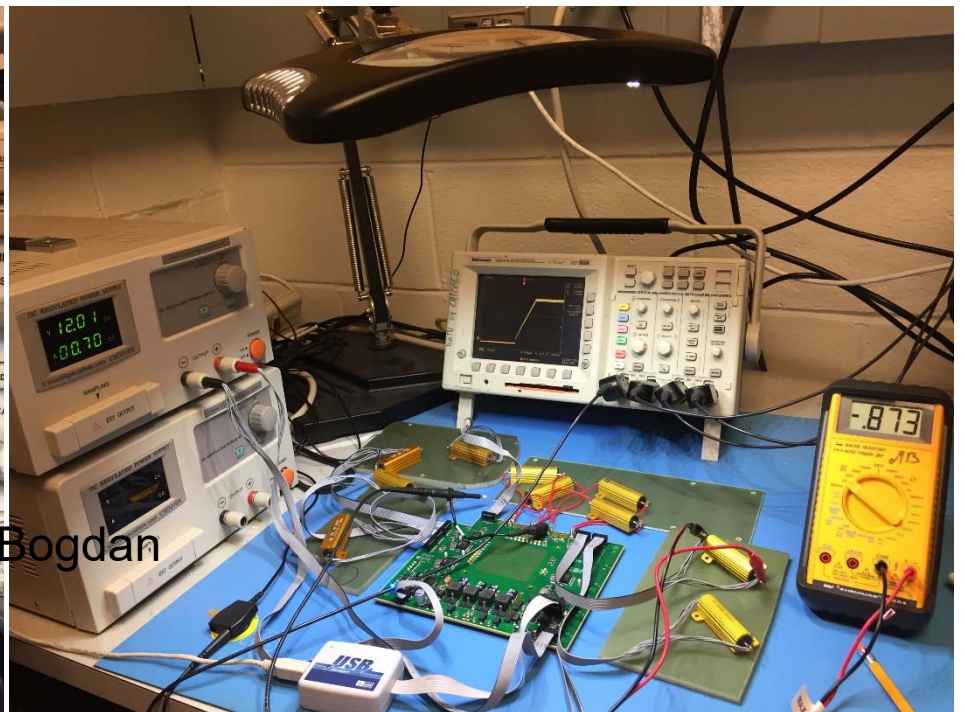
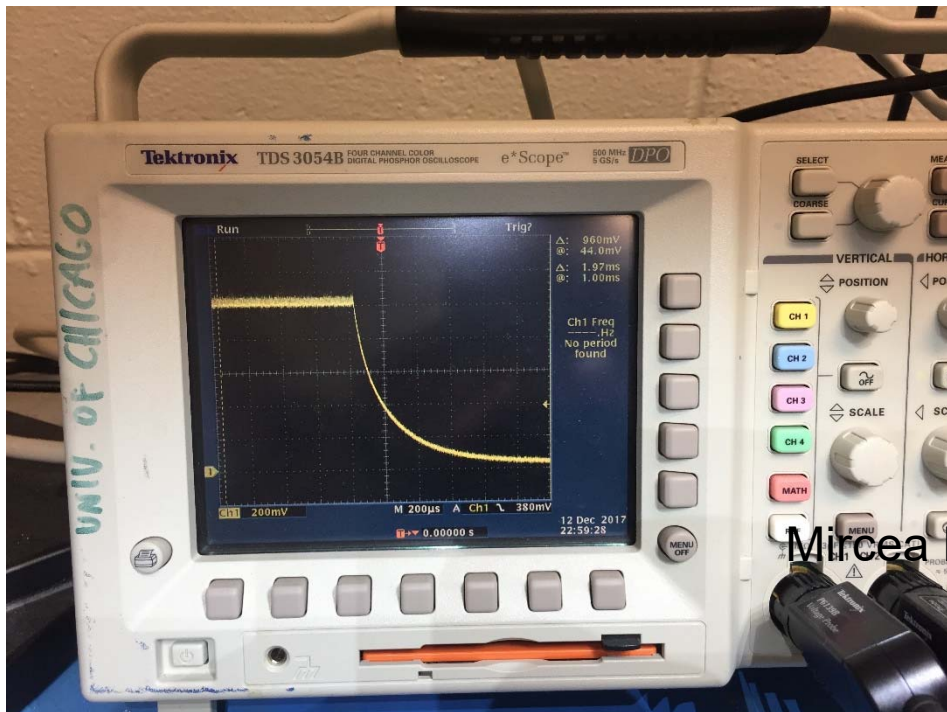
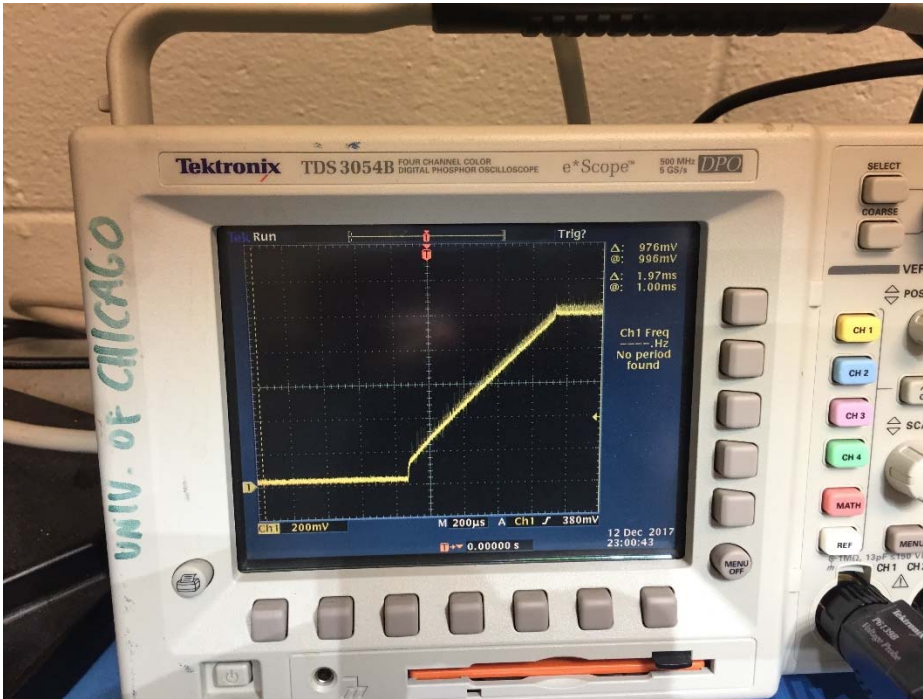


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TFM - VCCRL

- $V_{out} = 1.03V$
- $I_{out} = 4.35A$
- Efficiency = 88%
- $T_r \sim 800 \mu s$
- $T_f \sim 350 \mu s$

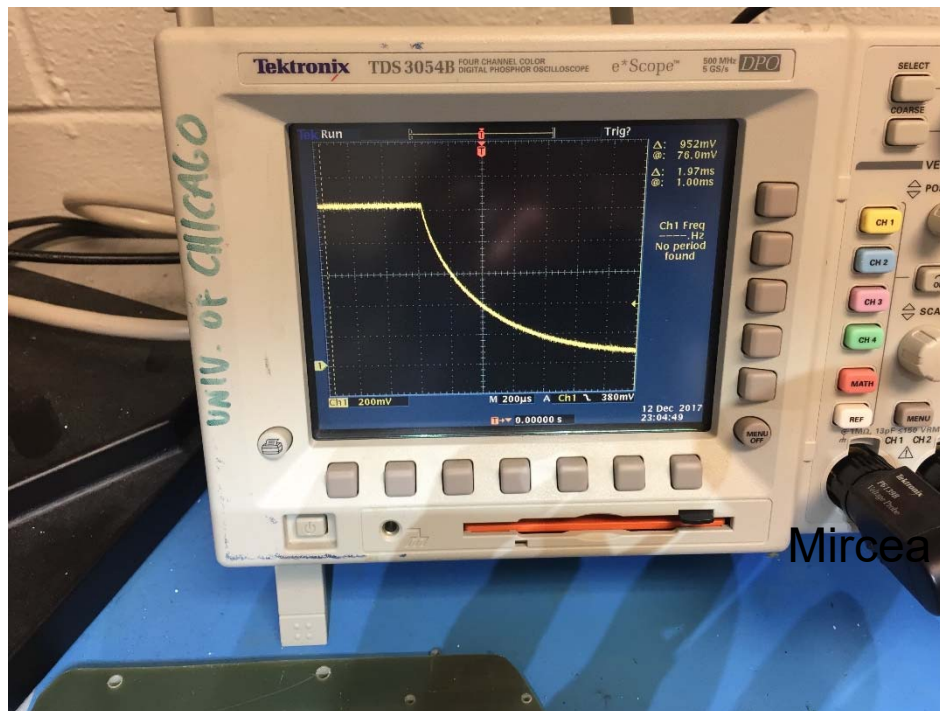
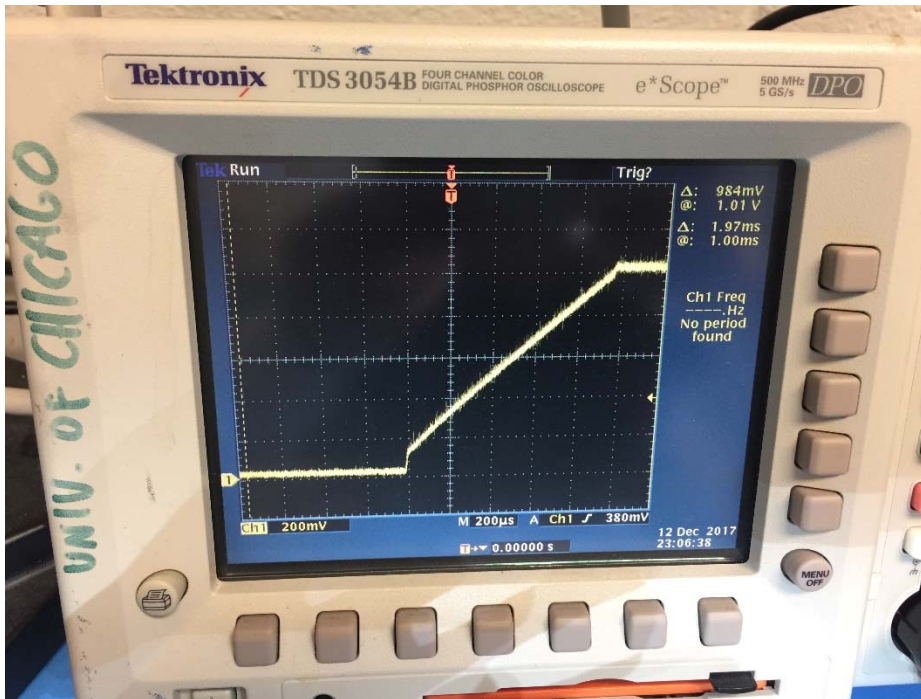


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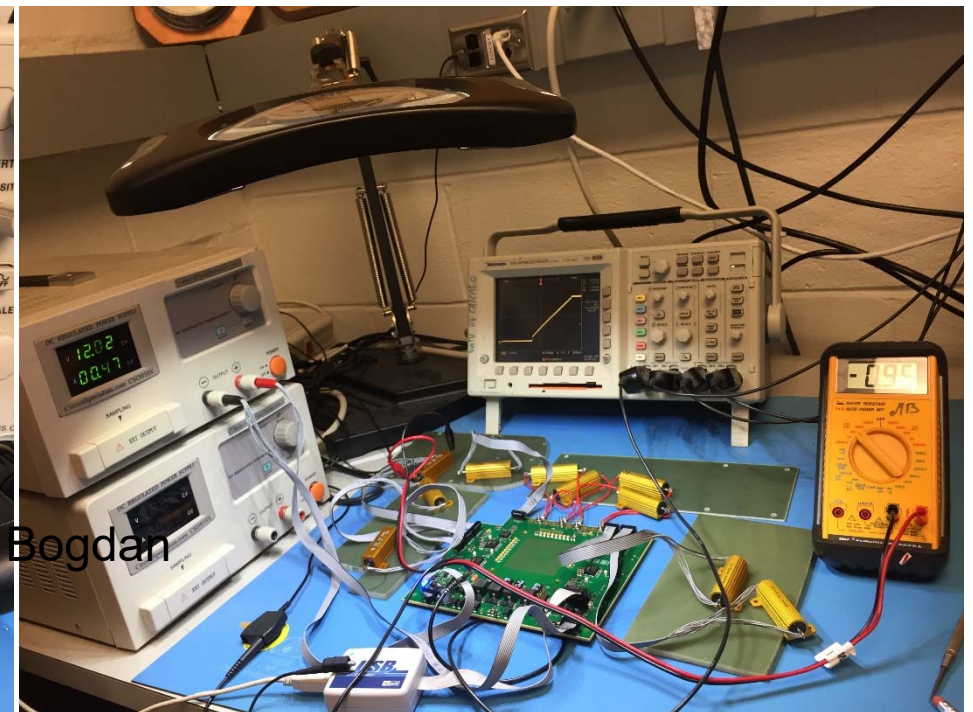
TFM - VCCT

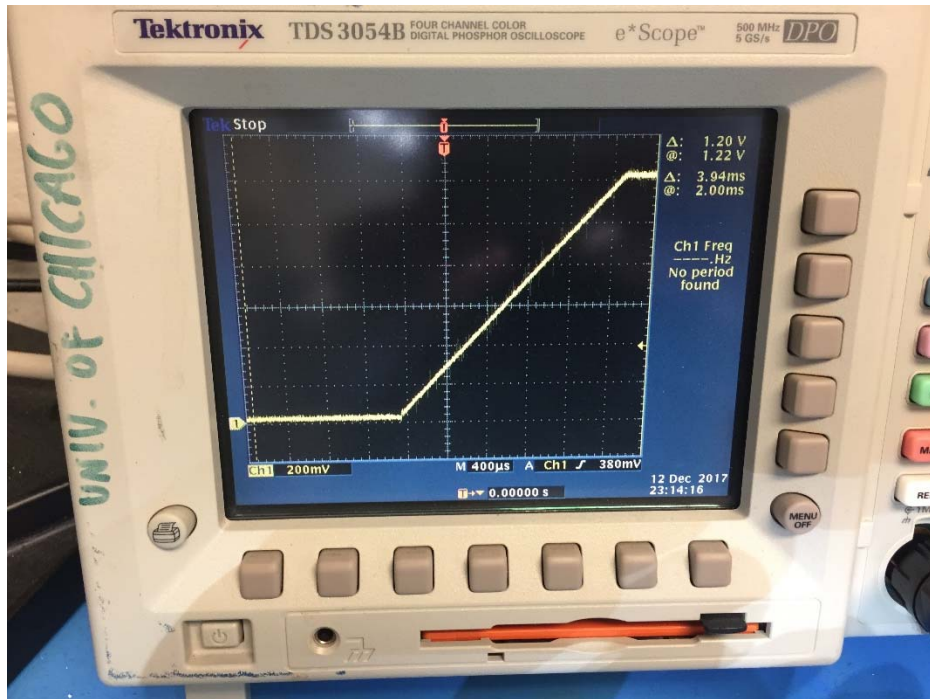
- $V_{out} = 1.03V$
- $I_{out} = 1.9A$
- Efficiency = 86%
- $T_r \sim 850 \text{ us}$
- $T_f \sim 1100 \text{ us}$

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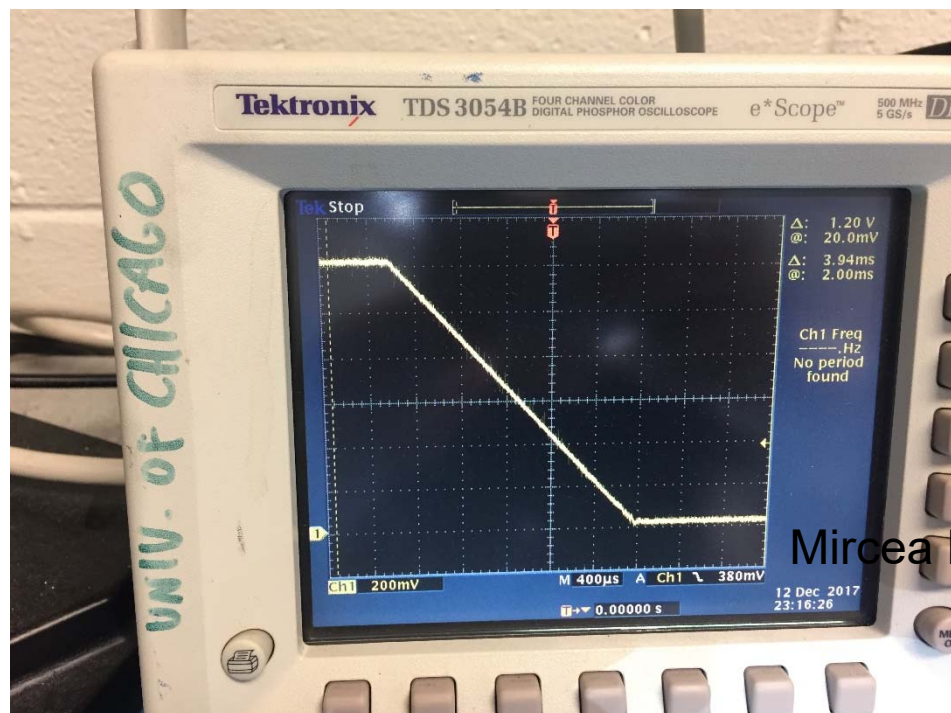




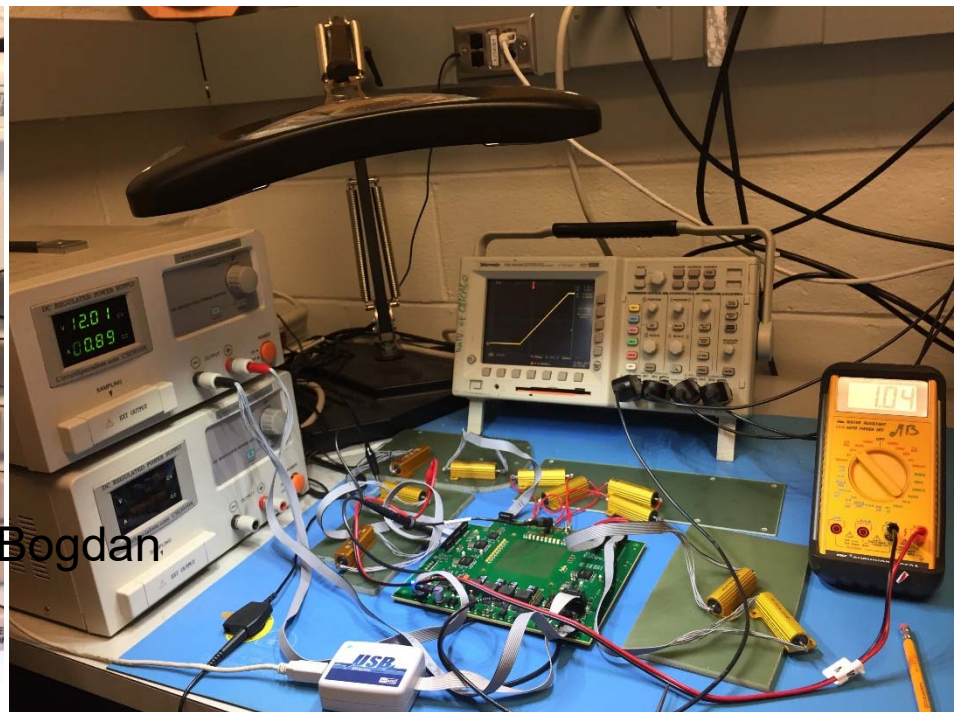
TFM - VCCIOUIB

- $V_{out} = 1.2V$
- $I_{out} = 5.2A$
- Efficiency = 85%
- $T_r \sim 1000 \mu s$
- $T_f \sim 1400 \mu s$

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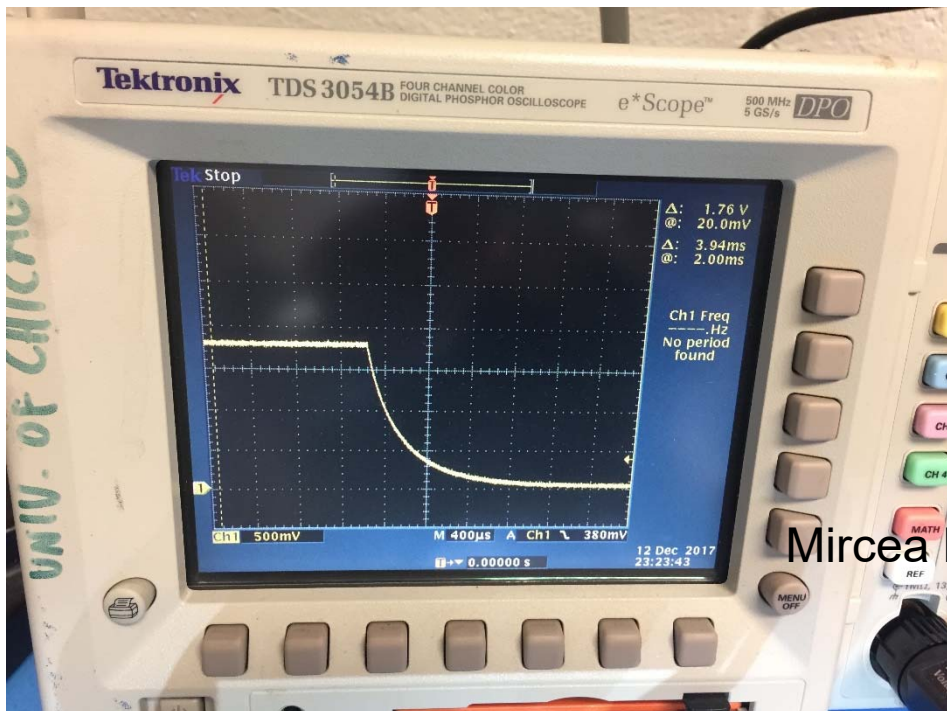
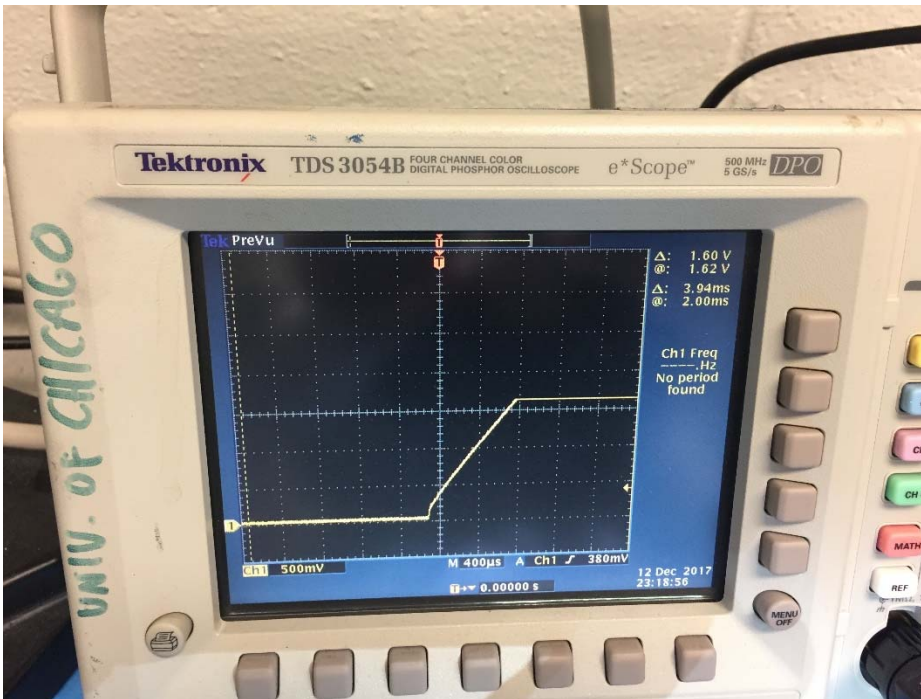


TFM - VCCH

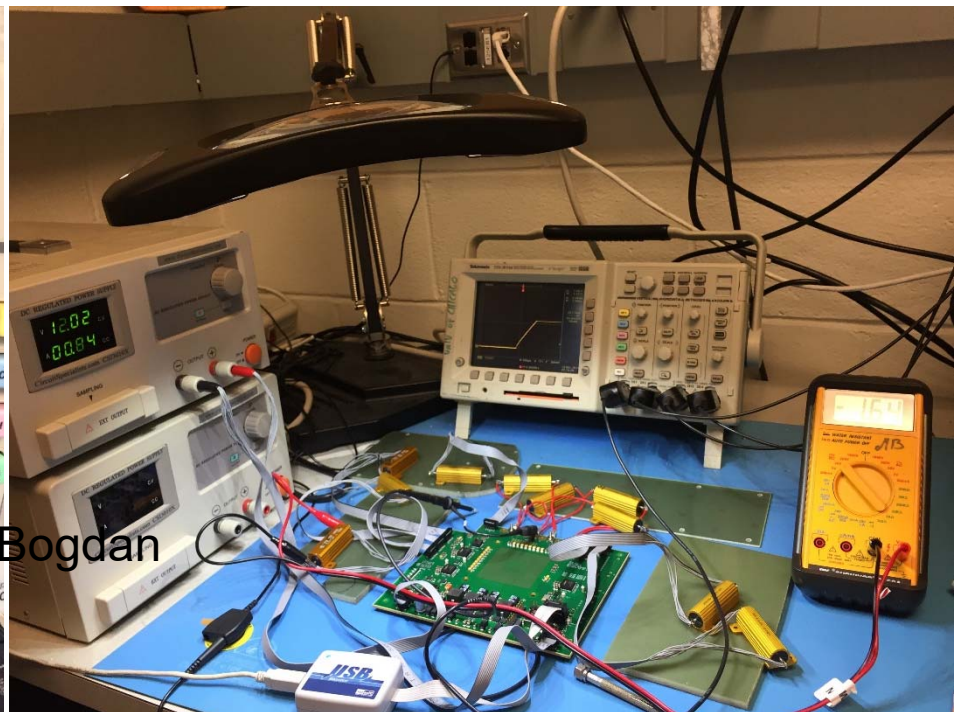
- $V_{out} = 1.8V$ (1.78V*)
- $I_{out} = 3.28A$
- Efficiency = 87%
- $T_r \sim 800 \mu s$
- $T_f \sim 1100 \mu s$

* Will adjust Resistors to make it 1.8V

EN63A0QI



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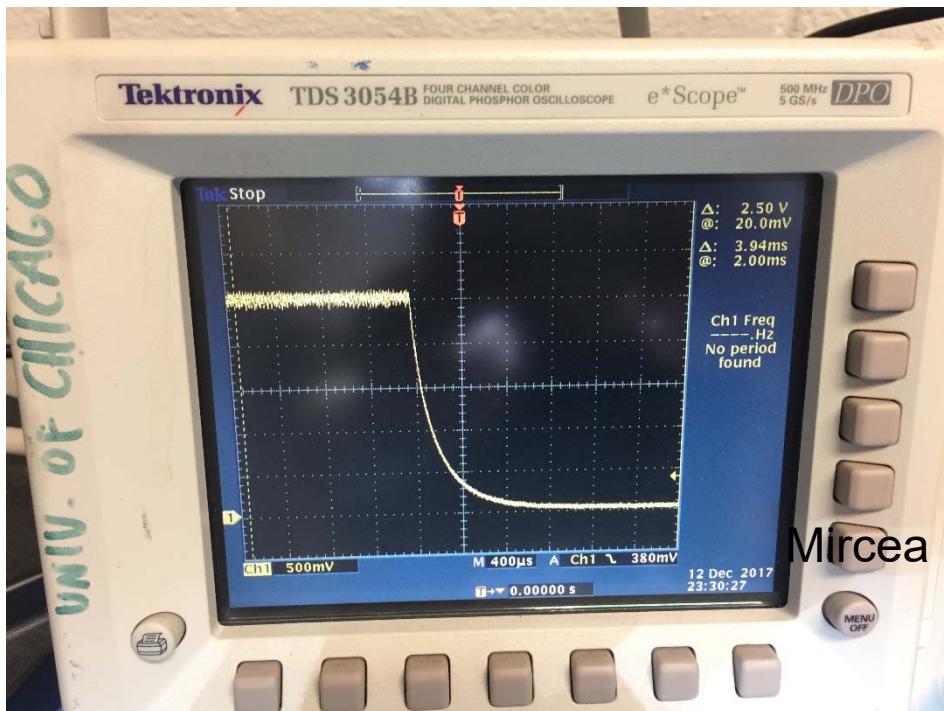
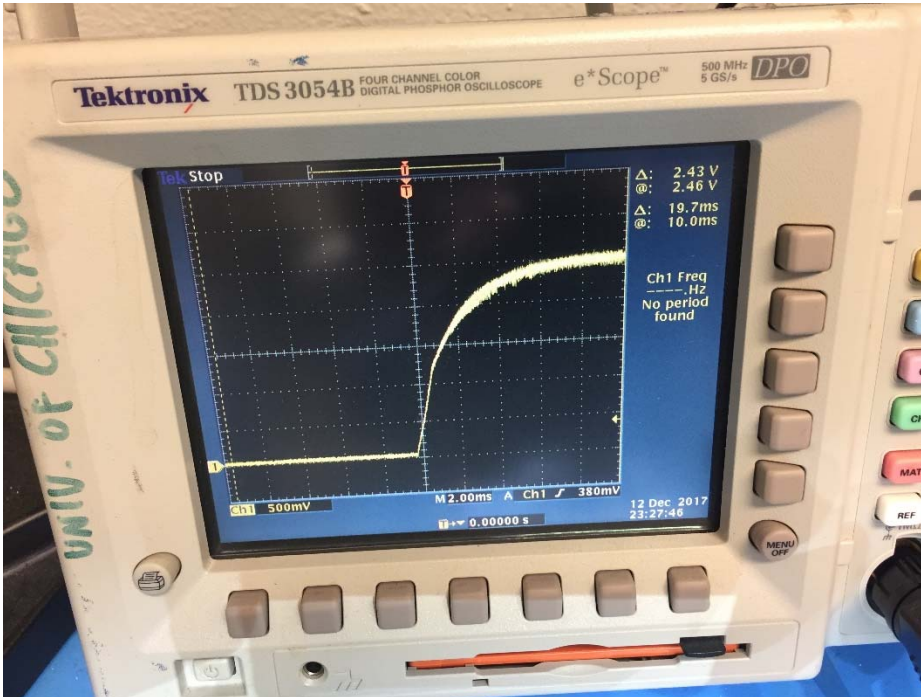


TFM - VCCM

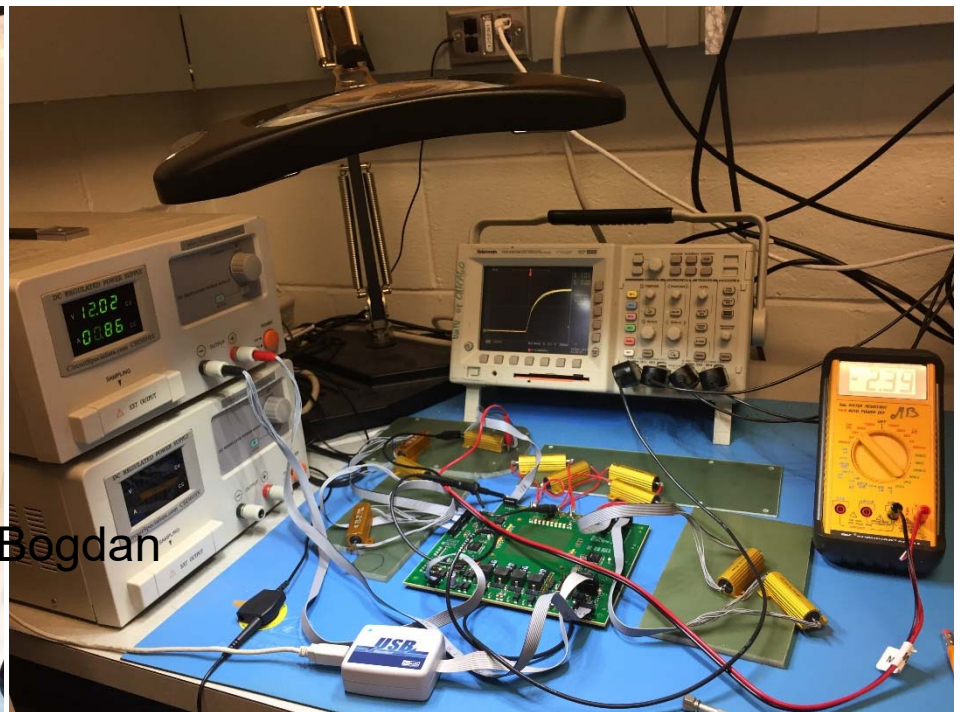
- $V_{out} = 2.5V$ (2.44V*)
- $I_{out} = 2.39A$
- Efficiency = 84%
- $T_r \sim 6$ ms
- $T_f \sim 800$ us

* Will adjust Resistors to make it 2.5 V

EN6362QI



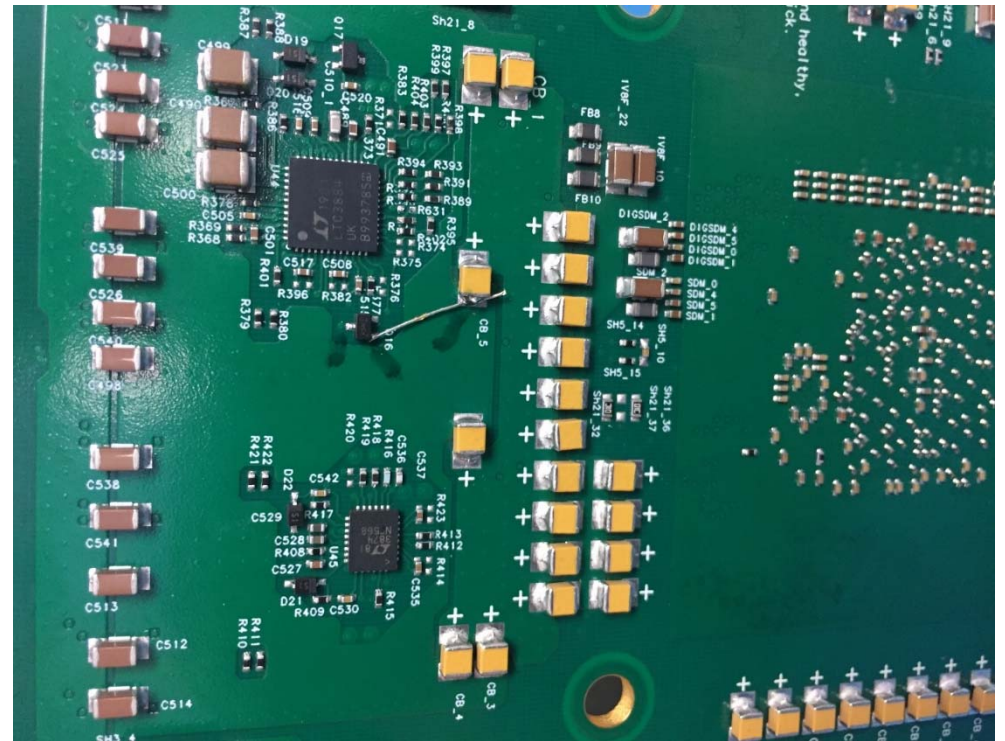
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TFM – Blue Wire



Broken contact

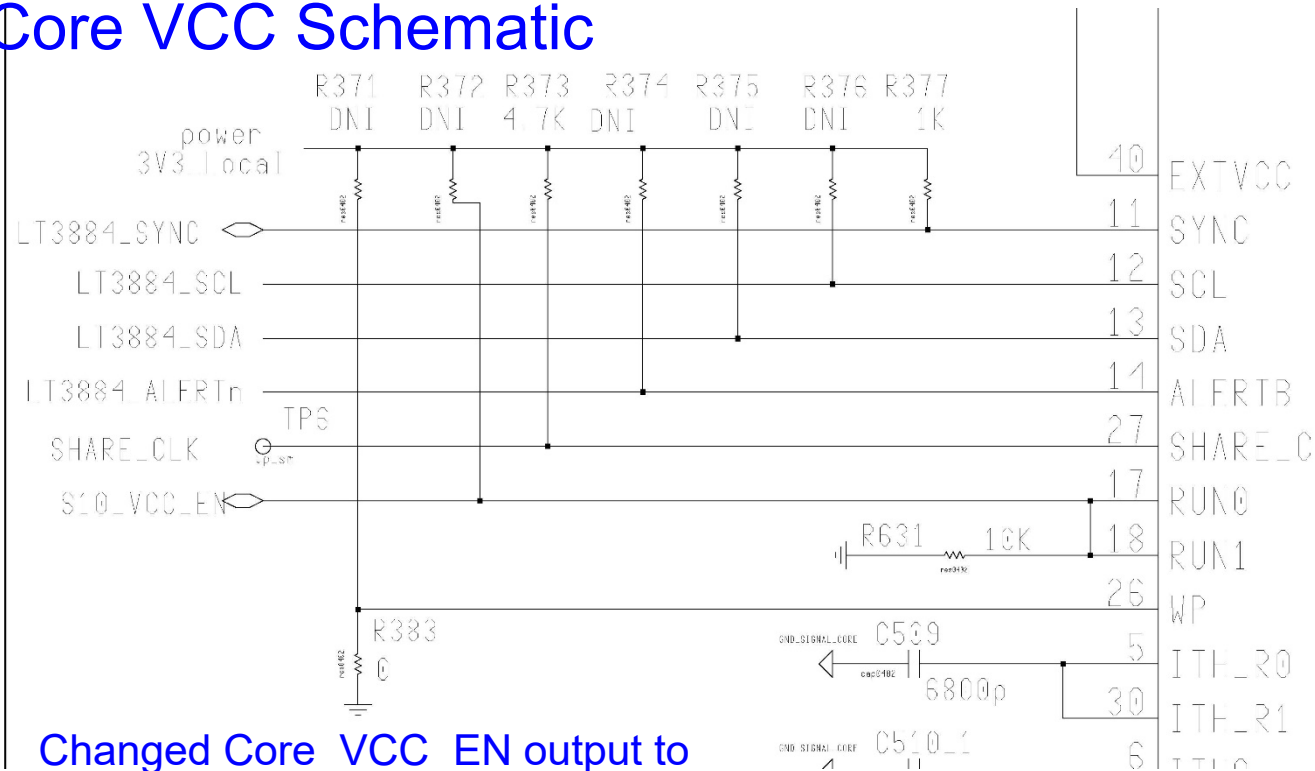


One Blue Wire

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TFM – Minor Change

Core VCC Schematic



- Changed Core_VCC_EN output to “Open Drain” in MAX10 Firmware
- Changed R631 from 10K to DNI
- Changed R372 from DNI to 10K

To Do:

Install 10K to GND on the POWER_ON line, to prevent Core DC/DC Convertor from starting before MAX10 is configured

LTC3884 Data Sheet Requirement:

RUN0/RUN1 (Pin 17/Pin 18, Pin 18/Pin 19): Enable Run Input and Output. Logic high on these pins enables the controller. An open-drain output holds the pin low until the LTC3884 is out of reset. This pin should be driven by an open-drain digital output. A pull-up resistor to 3.3V is required in the application.

TFM – To Do

- Test Power Supplies with Dynamic Loads
 - May have to change some capacitor values
- Output Voltage Ripple Measurement
 - May have to change some capacitor values
- Test Power Sequencing:
 - Will have to adjust Firmware
- Test TFM with TP Card
 -?
- Other Ideas?

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