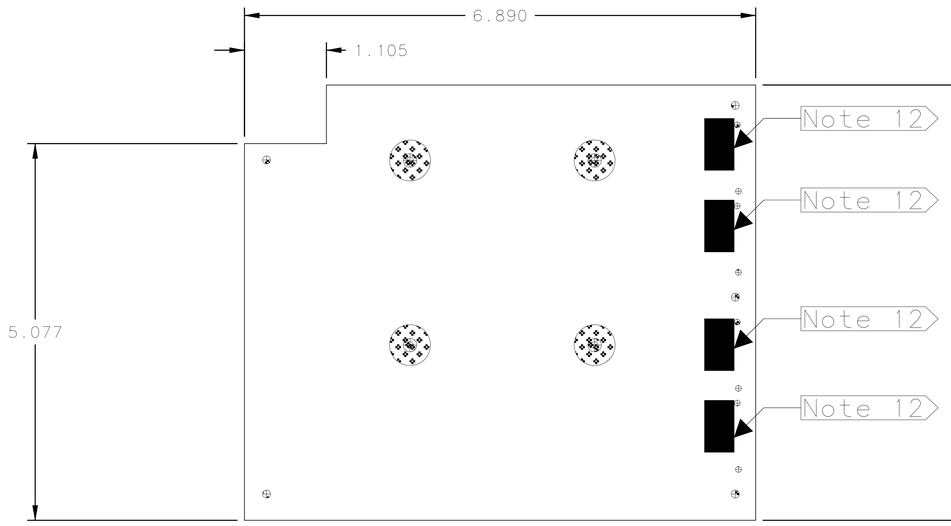
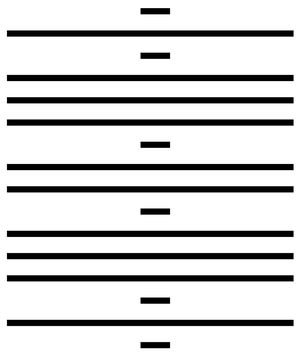


BOARD's HOLE SCHEDULE

FHS	COUNT	PLATED	COMMENT
.0077	38	YES	Note 4-1
.007874015	76	YES	
.008070866	49	YES	
.0081	1684	YES	
.0082	38	YES	Note 4-3
.008267716	58	YES	Note 4-4
.008661417	38	YES	Note 4-5
.009	612	YES	
.0091	2994	YES	
.0099	76	YES	
.0101	76	YES	Note 4-2
.019685039	300	YES	
.041	6	YES	
.078740157	8	NO	
.106299213	5	NO	
.149606299	1	YES	
.181102362	4	YES	

0. Use Document 2929-STK for PCB Stackup. No Stackup or Trace Width Changes shall be made without prior written approval.
1. Material: Magtron 6
2. Electroless Nickel/Immersion Gold plating; min 25 um Cu, 2.5-5 um Ni, 0.05-0.2 um Au.
   planarized and plated over with Copper and surface finish. The plated cap must adhere to the fill meterial after 1x550F solder shock.
3. Via Fill and Overplate is required. Vias in pad must be filled with Peters PP-2795 or equivalent solid fills,
4. Backdrilled Vias:
   4-1. Vias Backdrilled from Buttom Up - 38 pieces - These vias connect Layer 1 to Layer 14. Drill out and remove via stubs Layer 15-16.
   4-2. Vias Backdrilled from Bottom Up - 76 pieces - These vias connect Layer 1 to Layer 14. Drill out and remove via stubs Layer 15-16.
   4-3. Vias Backdrilled from Bottom Up - 38 pieces - These vias connect Layer 1 to Layer 3. Drill out and remove via stubs Layer 4-16.
   4-4. Vias Backdrilled from Top Down 38 pieces - These vias connect Layer 14 to Layer 16. Drill out and remove via stubs Layer 1-13.
   4-5. Vias Backdrilled from Top Down 38 pieces - These vias connect Layer 3 to Layer 16. Drill out and remove via stubs Layer 1-2.
5. Silkscreen on Both Sides. Discard any writings smaller than 10 mils.
6. Impedance 50 Ohm for all 5mil single ended traces, and 95 Ohm for all 5/6 mil differential traces.
7. FHS tolerances : +/- 0.003" unless specified otherwise.
8. Board Thickness: 0.095"+/-0.008"
9. Trace Width=5mils. Min Crearance = 4 mils.
10. 1 oz Copper for Layers: 1,2,4,5,6,8,,9,11,12,13,15,16; 1/2 oz Copper for Layers 3,7,10,14.
11. Remove all non-functional inner layer pads for pins and vias.
12. There are 4 Compression Pad Array Fields on Bottom Side of PCB, each with 168 pads and with the following Specs:
    12-1. Compression PCB Pad Coplanarity must be 0.002 Inches Maximum across each array field.
    12-2. Compression Side Pad Plating must be 0.00003 Inches Gold with Hardness of 130-200 Knoop per ASTM B488, Type 2 C.

Layer Order:



1 Oz	1.	Signal 1, Top
1 Oz		Ground
0.5 Oz		Signal
1 Oz		Ground
1 Oz		Power
1 Oz		Power
0.5 Oz		Signal
1 Oz		Power
1 Oz		Power
0.5 Oz		Signal
1 Oz		Power
1 Oz		Power
1 Oz		Ground
0.5 Oz		Signal
1 Oz		Ground
1 Oz	16.	Signal 6, Bottom

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.008
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M. Bogdan	10/2/2019
CHECKED M. Bogdan	10/2/2019
ISSUED	

THE UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
TFM
Specification Drawing

SIZE | FSCM NO. | DWG. NO. 2929 | REV. A

SCALE 1/2 | SHEET 1 of 1

THIS SHEET IS COMPUTER GENERATED