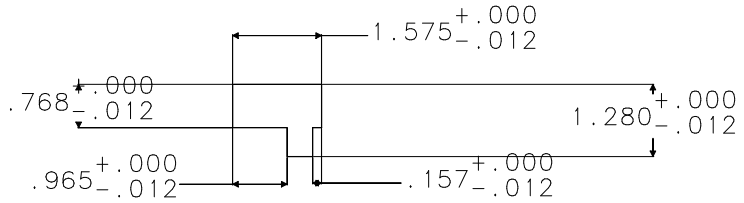


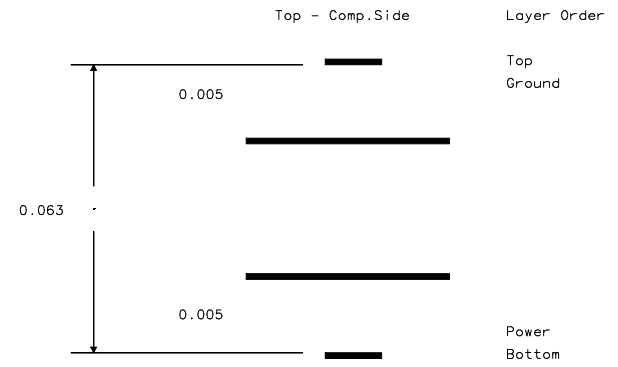


Board Characteristics

0. All dimensions are given in inches unless specified otherwise.

2. Minimum trace width: 0.006" and clearence: 0.005" on Signal_1,6 (Top and Bottom);
3. Minimum trace width and clearence: 0.005" on Signal_2,3,4,5,7,8,9,10 (all stripline);
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)

Apply Solder Mask over bare copper.

6. Board Thickness: 0.0

8. Silkscreen on Component and Solder Sides.

10. FHS tolerances: +/- 0.003
11. Interlayer spacing as specified

12. Zc=50 Ohm +/- 5 Ohm
Perform TDR test for all signal layers.
Present TDR test results for all signal layers.

BOARD's DRILL SCHEDULE

| DRILL SYMBOL | DRILL SIZE | COUNT | PLATED | Tolerance | COMMENT |
|---|---|---|---|---|---|
| ○ | .0098425197 | 9 | YES | --- | |
| ⊞ | .014 | 75 | YES | --- | |
| ⌀ | .041 | 3 | YES | --- | |
| ⊟ | .042 | 20 | YES | --- | |
| ⊖ | .13779528 | 1 | NO | --- | |

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

| APPROVALS | | DATE |
|---|---|---|
| DRAWN | M.Bogdan | 12/8/11 |
| CHECKED | M.Bogdan | 12/8/11 |
| ISSUED | | |

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Jitter Cleaner
Specification Drawing

SIZE B | FSCM NO. | DWG. NO. 2774 | REV. A

SCALE 1/1 | SHEET

IS SHEET IS COMPUTER GENERATED