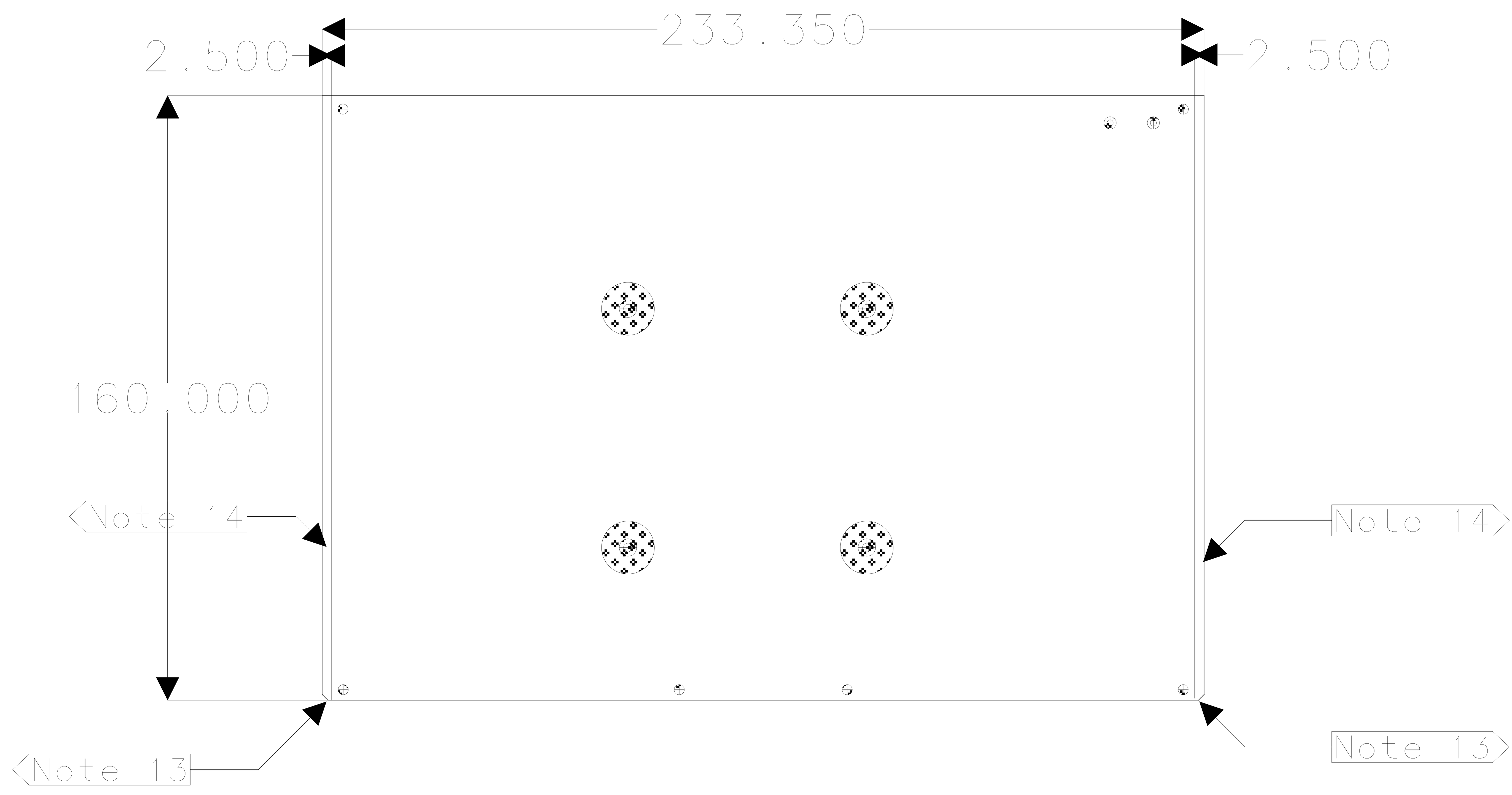
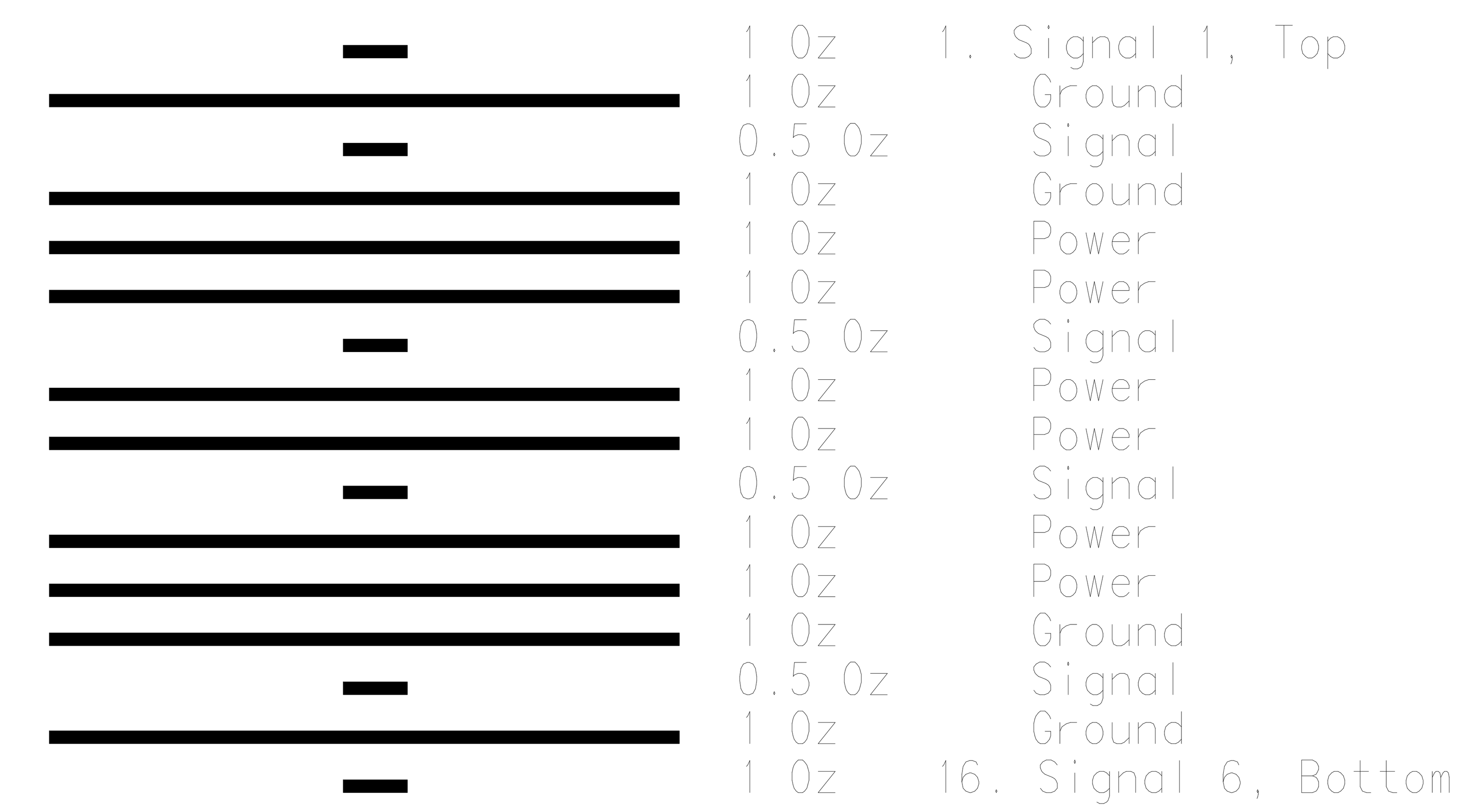


BOARD's HOLE SCHEDULE [mm]

FHS	COUNT	PLATED	COMMENT
.2	487	YES	
.20574	1877	YES	
.2286	1440	YES	
.23114	4260	YES	
.5	372	YES	
.6096	16	YES	
1.0414	412	YES	
1.05	78	YES	
1.2	14	YES	
1.4478	6	YES	
1.55	18	YES	
1.6	6	YES	
2	4	YES	
2.2606	7	YES	
2.54	2	YES	
2.6924	4	NO	
2.7	2	NO	
3.24993	2	YES	
4.6	4	YES	

Layer Order:



1 Oz	1. Signal 1, Top
1 Oz	Ground
0.5 Oz	Signal
1 Oz	Ground
1 Oz	Power
1 Oz	Power
0.5 Oz	Signal
1 Oz	Power
1 Oz	Power
0.5 Oz	Signal
1 Oz	Power
1 Oz	Power
1 Oz	Ground
0.5 Oz	Signal
1 Oz	Ground
1 Oz	16. Signal 6, Bottom

0. Stackup as per 2959-STK
1. Material: Magtron 6
2. Electroless Nickel/Immersion Gold plating; min 25 um Cu, 2.5-5 um Ni, 0.05-0.2 um Au.
3. Via Fill and Overplate is required. Vias in pad must be filled with Peters PP-2795 or equivalent solid fills, planarized and plated over with Copper and surface finish. The plated cap must adhere to the fill meterial after 1x550F solder shock.
5. Silkscreen on Both Sides. Discard any writings smaller than 10 mils.
6. Impedance 50 Ohm for all 5mil single ended traces, and 95 Ohm for all 5/5 mil differential traces.
7. FHS tolerances : +/- 0.003" unless specified otherwise.
8. Board Thickness: 0.095"+/-0.008"
9. Min Trace Width=4.5mils. Min Crearance = 4 mils.
10. 1 oz Copper for Top, Bottom and Power Layers; 1/2 oz Copper for all Internal Signal Layers
11. Remove all non-functional inner layer pads for pins and vias.

13. 45 Degree Chamfer
14. Mill 2.5mm on two edges of the board, on bottom side only, to a remaining thickness of 0.063' +/- 10%.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS .008 ANGLES DO NOT SCALE DRAWING	CONTRACT NO.	THE UNIVERSITY OF CHICAGO ELECTRONICS DEVELOPMENT GROUP
TREATMENT	APPROVALS / DATE	TITLE: OFC-2 Specification Drawing
FINISH	DRAWN M. Bogdan 11/17/20	SIZE / FSCM NO. / DWG. NO. 2959 / REV. A
SIMILAR TO / ACT. WT / CALC WT	CHECKED M. Bogdan 11/17/20	SCALE 1/2 / SHEET 1 of 1
	ISSUED	