

4

3

DRG. NO. B-2499

SH 1 REV. A

1

D

D

Layer Order

1. Signal_1

2. Power_1 VCC

3. Signal_2

4. Signal_3

5. Power_4 GND

6. Signal_4

0.062"
+/- .008"

0.034"

0.007"

0.005"

C

C

149.000±.100

mm

B

B

Board Characteristics

1. Dimensions are given in inches and mm;
2. Material FR4,
3. Min trace width: 0.006" on all layers;
4. Min. clearance: 0.006" on all layers;
5. 1 oz copper for top, bottom and power layers;
6. Electroless Nickel/Immersion Gold plating. Apply soldermask;
7. FHS tolerances: 0.002";
8. Board thickness and inter-layer spacing as specified;
9. Silkscreen on both sides;
10. Trace impedance: 55 Ohm +/-5 Ohm for 0.006" traces on all layers;

B

B

BOARD'S DRILL SCHEDULE

FHS [Inches]	COUNT	PLATED	COMMENT
.02	365	YES	
.041	75	YES	
.042	80	YES	
.0551	4	NO	
.057	2	YES	
.1063	8	NO	

A

A

QUESTIONS SPECIFIED DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED. DECIMALS .XX

ON NOT SCALE DRAWINGS

CONTRACT NO. TITLE The University of Chicago Electronics Development Group

APPROVALS: DRAM M. Bogdan 11/12/02 DATE 11/12/02

CHECKED BY: M. Bogdan

FINISH: SCALE B SIZE: 1/1

ISSUED: 11/12/02

THIS SHEET IS COMPUTER GENERATED

4

3

2

1