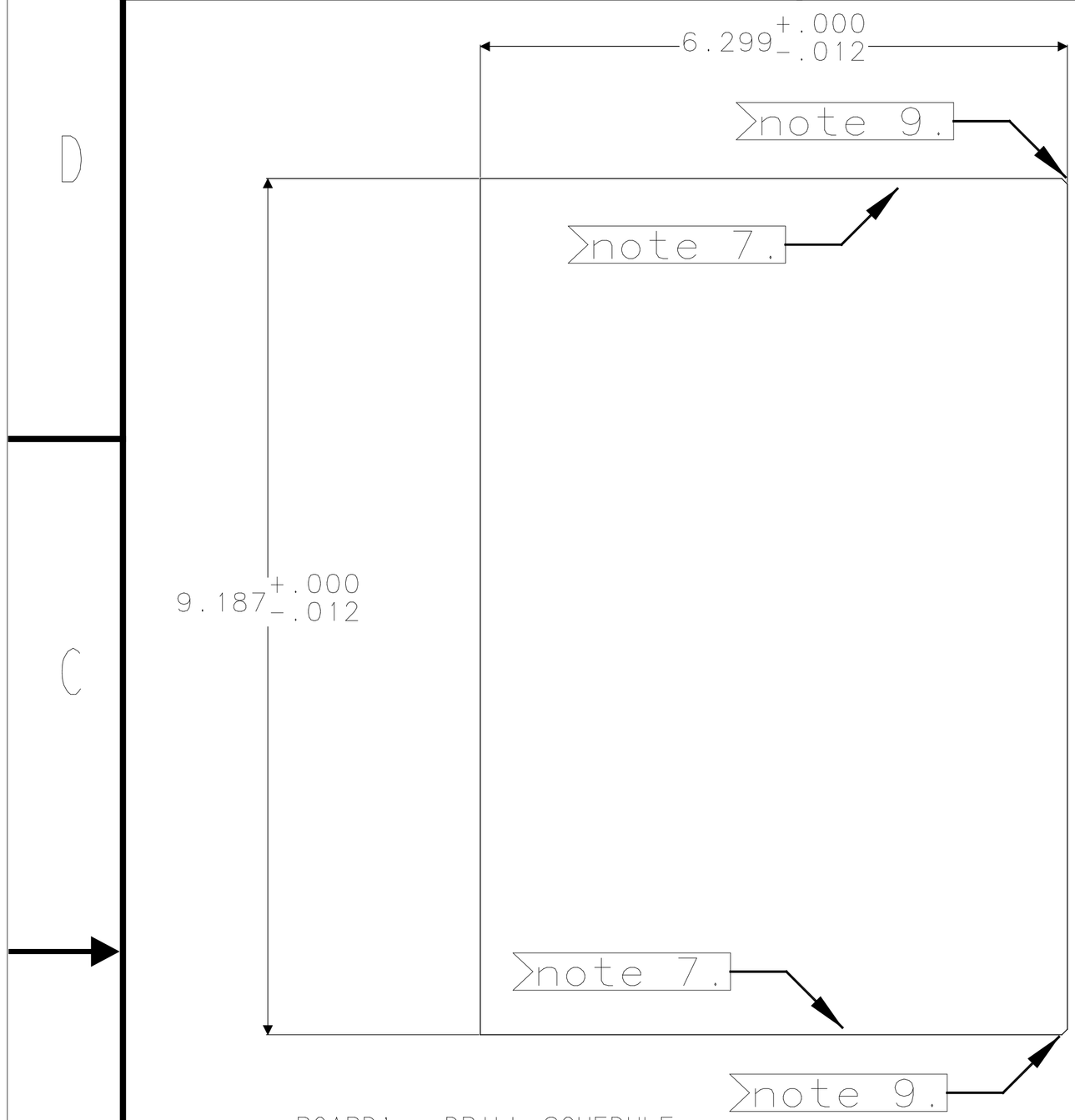
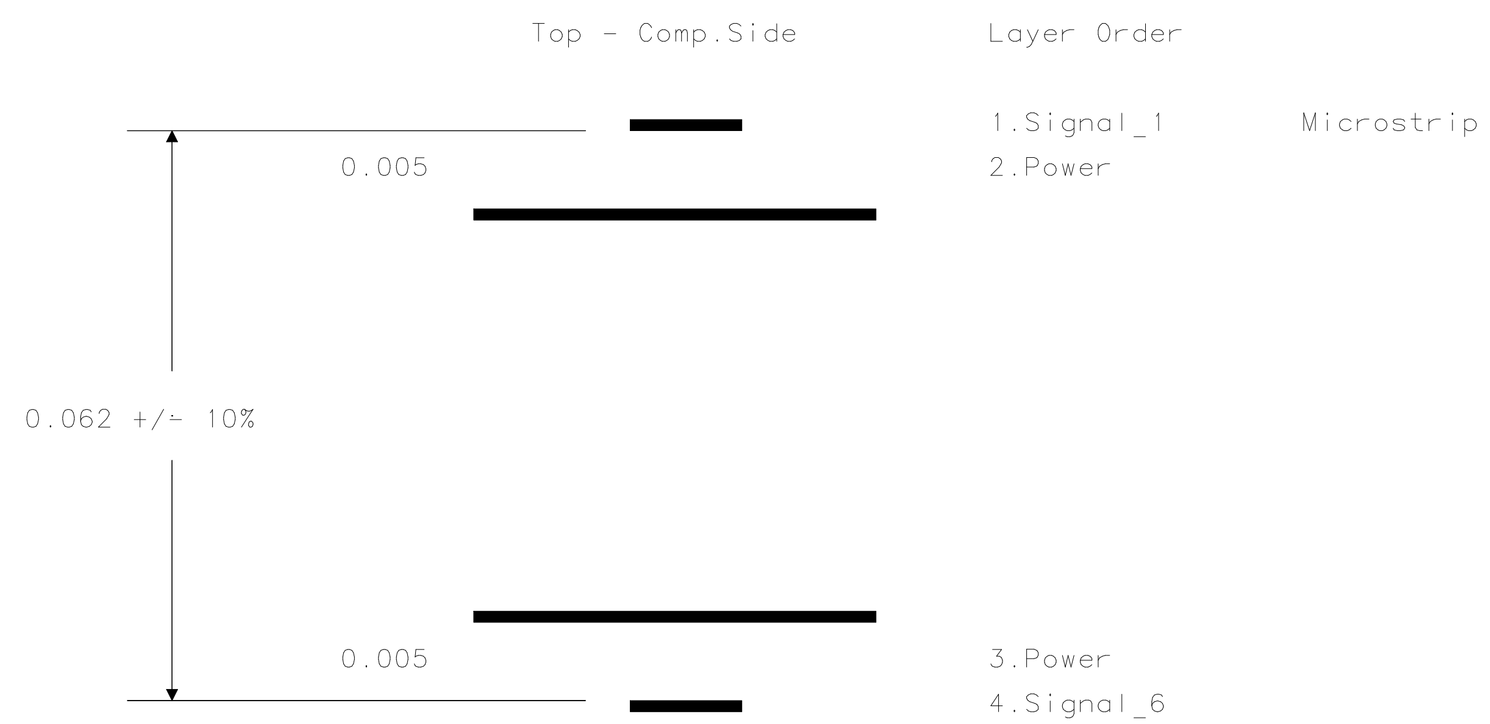


BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.014	283	YES	---	
⊞	.035	40	YES	---	
⌀	.041	402	YES	---	
⊟	.052	25	YES	---	
⊖	.057	21	YES	---	
◫	.062992126	10	YES	---	
⊕	.106	6	NO	---	
□	.12795276	10	YES	---	
	.15	2	NO	---	



Board Characteristics - 4 LAYER BOARD

0. All dimensions are given in inches unless specified otherwise.

2. Minimum trace width: 0.006" and clearence: 0.005" on Signal_1,6 (Top and Bottom);
3. Minimum trace width and clearence: 0.005" on Signal_2,3,4,5,7,8,9,10 (all stripline);
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)

5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.062 +/- 10%

8. Silkscreen on Component Side
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.003 unless specified otherwise.
11. Interlayer spacing as specified

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	3/27/2018
CHECKED M.Bogdan	3/27/2018
ISSUED	

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
NIM/LVDS Translator
Specification Drawing

SIZE B | FSCM NO. | DWG.NO. 2914 | REV. A

SCALE 1/2 | SHEET

THIS SHEET IS COMPUTER GENERATED