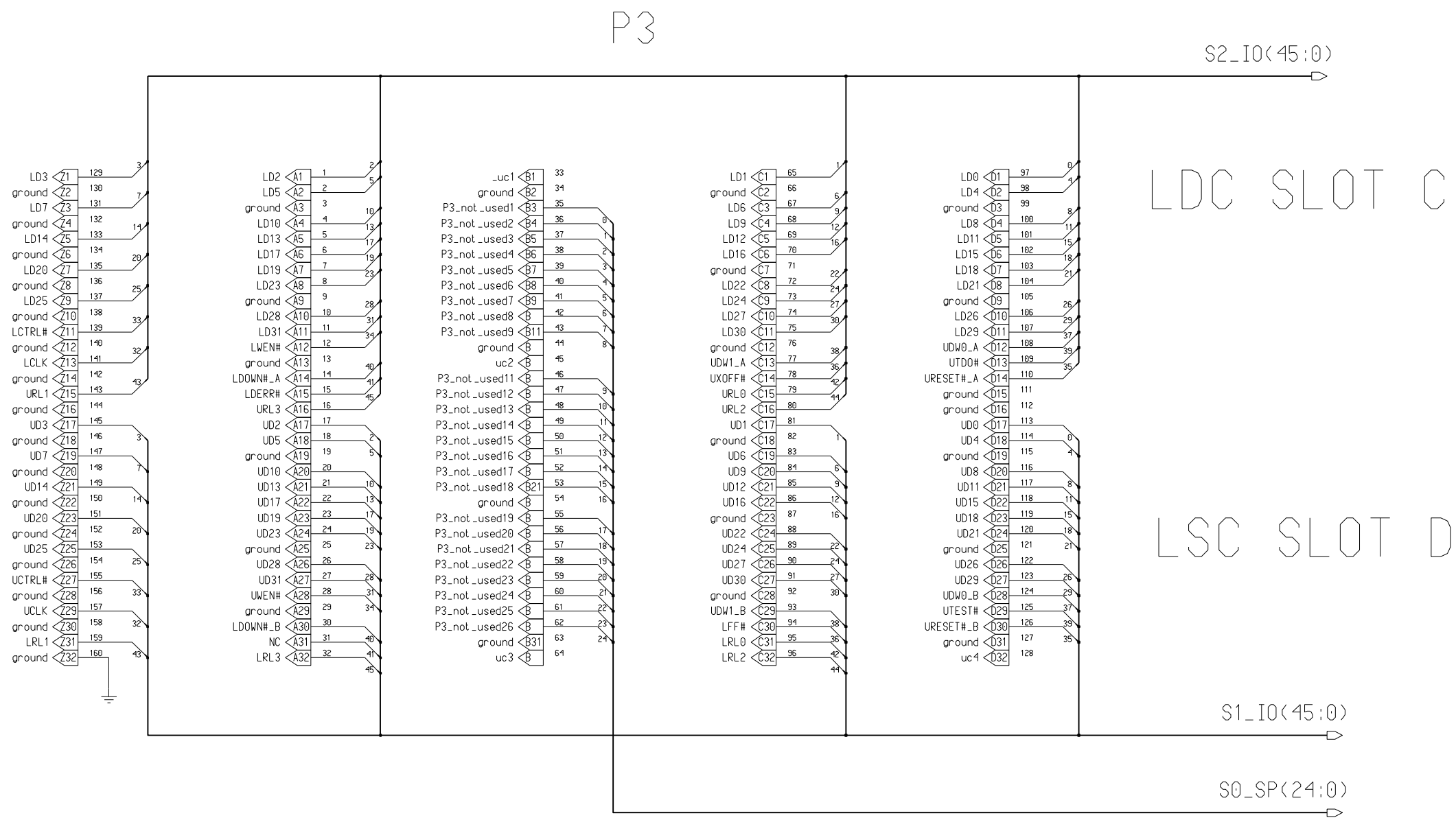
5-row P3 connector map to one SLINK LDC and one LSC (use P2-type backplane).
the signals into control FPGA are mapped in such a way to be consistent with the mezzanine card connector, to make life easier in firmware

The 32 data bits are mapped to S_IO(31:0), other signals are mapped to higher bits. the mapping is similar for both LDC and LSC signals.



DATE	REVISION DESCRIPTION

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
Level2 Pulsar / P3

SHEET 14 OF 25
DATE 5/15/2002
DRWN MB/TL

C-2501
REV A