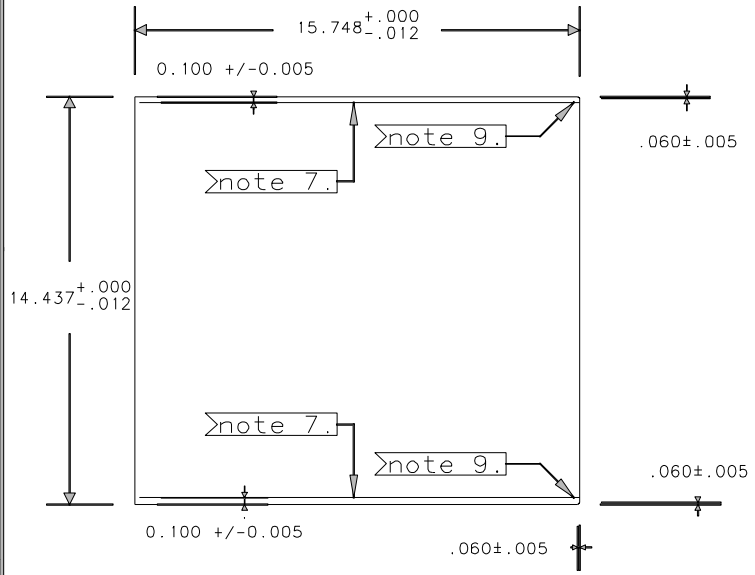

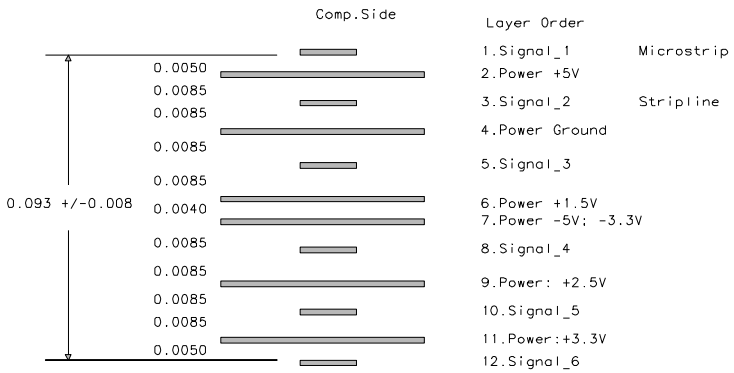

BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Tolerance	COMMENT
○	.014	1560	YES	---	
⊞	.018	2724	YES	---	
⊕	.02	351	YES	---	
⊟	.0236	387	YES	Note 12.	Note 12.
⊖	.035	272	YES	---	
◫	.041	733	YES	---	
⊕	.042	60	YES	---	
□	.05	1	YES	---	
	.052	20	YES	---	
	.057	54	YES	---	
	.095	12	YES	---	
	.106	9	NO	---	
	.113	6	NO	---	
	.12	8	YES	---	
	.16	3	YES	---	

Board Characteristics

0. All dimensions are given in inches unless specified otherwise.
1. Material FR4 with Tg>170C, E.g. FR406
2. Minimum trace width and clearence: 0.006" on Signal_1,6 (Top and Bottom);
3. Minimum trace width and clearence: 0.005" on Signal_2,3,4,5 (all stripline traces);
4. 1 oz copper for all power layers and for Signal_1,2 (Top and Bottom)
   1/2 oz copper for Stripline trace layers (Signal_2,3,4,5).
5. Immersion Gold over copper, with min. Ni: 2.5-5 um; Au: 0.05-0.2 um.
   Apply Solder Mask over bare copper.
6. Board Thickness: 0.093 +/- 0.008
7. Mill the Top and Bottom of board on the solder side to a thickness of 0.062" +/- 0.008
8. Silkscreen on Component and Solder Sides.
9. 45 degree chamfer.
10. FHS tolerances: +/- 0.002 unless specified otherwise.
11. Interlayer spacing as specified
12: This is a pressfit technology thru hole with the following specs:
   12-1. Finished plated hole size: 0.59 - 0.65 mm.
   12-2. Drilled hole size: 0.7mm +/- 0.02mm
   12-3. Min. Thickness of thru hole plating: Cu: 25 μm; Ni: 2.5-5 μm; Au: 0.05-0.2 μm.
13. Zc=60 Ohm +/- 5 Ohm for 0.005" stripline and 0.006" microstrip traces on all layers.
13a. Zdiff=105 Ohm +/- 5 Ohm for 0.005"(0.005" apart) stripline and
   0.006" (0.006" apart) microstrip traces on all layers.
   Perform TDR test (Zc and Zdiff) for all signal layers.
   Present TDR test results for all signal layers.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
.XX
.XXX
DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN M.Bogdan	6/3/04
CHECKED M.Bogdan	6/3/04
ISSUED	

TREATMENT

FINISH

SIMILAR TO | ACT. WT | CALC WT

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
TDC Board
Specification Drawing

SIZE B | FSCM NO. | DWG. NO. A - 2530 | REV B

SCALE 1/4 | SHEET

THIS SHEET IS COMPUTER GENERATED