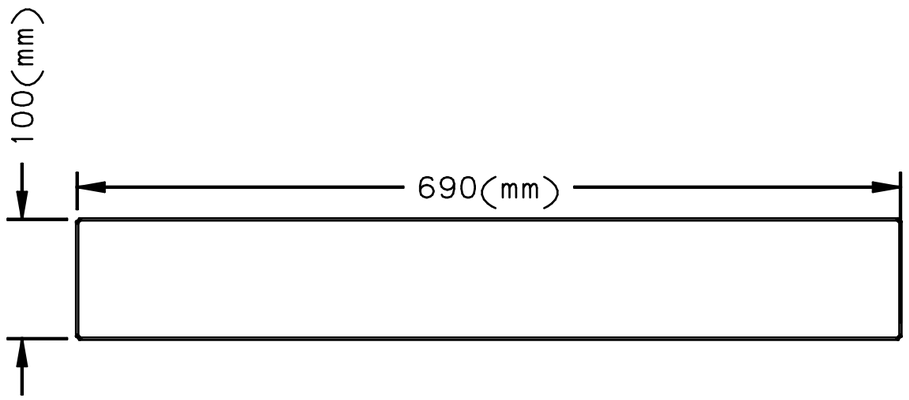
B-2800 BOARD DIMENSION



BOARD's DRILL SCHEDULE

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
O	.01	3141	YES	---
⊞	.015	180	YES	---
⊕	.02	10	YES	---
⊟	.035	480	YES	---
⊖	.04	8	YES	---
◫	.041	14	YES	---
⊕	.048	124	YES	---
□	.05	26	YES	---
	.059	48	YES	---
	.1378	12	YES	---

B-2800 BOARD SPECIFICATIONS

1. Board Layers: 14
2. Layer Stack Order:

Layer1 (Artwork_1): Top comp layer (Signal_1) 1 oz, Zdiff=100 ohms
Layer2 (Artwork_2): Power plane (AGND_A, AGND_B), 2oz
Layer3 (Artwork_3): Inner Signal_3, 1oz, Zdiff=100 ohms
Layer4 (Artwork_11): Power plane (Ground), 2oz
Layer5 (Artwork_4): Inner Signal_5, 1oz, Zdiff=100 ohms
Layer6 (Artwork_5): Power plane (P5V_A, P5V_B), 2oz.
Layer7 (Artwork_6): Power plane (P10V_A, P10V_B, P1V2_A, P1V2_B), 2oz
Layer8 (Artwork_7): Power plane (P2V5_A, P2V5_B, P1V8A_A, P1V8A_B), 2oz
Layer9 (Artwork_8): Power plane (N5V_A, N5V_B), 2oz
Layer10 (Artwork_9): Inner Signal_4, 1oz, Zdiff=100 ohms
Layer11 (Artwork_11): Power plane (Ground), 2oz
Layer12 (Artwork_10): Inner Signal_6, 1oz, Zdiff=100 ohms
Layer13 (Artwork_11): Power plane (Ground), 2oz
Layer14 (Artwork_12): Bottom comp layer (Signal_2) 1 oz, Zdiff=100 ohms

3. Apply silkscreen on Top component side:
   Artwork_13: Top silkscreen.
   Artwork_14: Bottom silkscreen.
4. Apply solder mask over bare copper on both side:
   Artwork_15: Top solder mask
   Artwork_16: Bottom solder mask
5. Material: FR4, TG > 170C
6. Board thickness: 0.090" +/- 0.010".
7. Diff traces impedance of all signal layers should be controlled at 100 ohms +/-5%.
8. Diff trace/gap/trace laid out in 5/5/5 mils, can be adjusted by PCB makers for impedance control.
9. Minimum Trace/gap = 5/5 mils
10. Copper thickness for signal layers before plating is 1oz.
11. Copper thickness for all power layers is 2oz.
12. Board finish type: Immersion gold.
13. Solder masking for all bare copper
14. All dimensions are in inches unless otherwise noted.
15. Send back stack-up parameters and suggusted trace/gap for impedence control for approval.
16. Send back gerber plots (pdf is accetable) for approval.

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SPC# B-2800
ASM# B-2801

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
B-2800 specifications

SHEET 1 OF 1
DATE 04/15/13
DRAWN F.TANG

B- 2800
REV 1.0