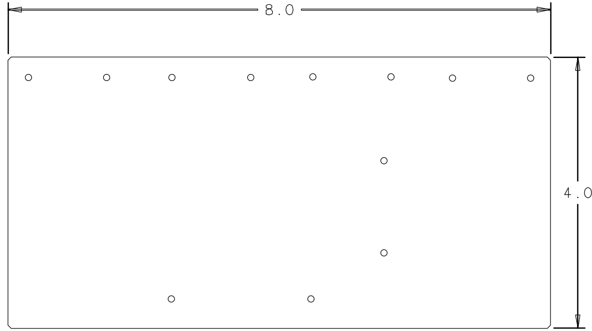
A2524 Board Size (mm)



BOARD SPECIFICATIONS

1. Board Layers: 8
2. Layer Stack Order:

Layer1 (Artwork_1): Top component layer (Signal_1), 0.5oz, Tz=50 ohm
Layer2 (Artwork_2): Power_1 (VCC), 1oz
Layer3 (Artwork_3): Power_3 (GROUND), 1oz
Layer4 (Artwork_4): Power_4(VCC5V), 1oz
Layer5 (Artwork_5): Power_2 (VCC1V8), 1oz
Layer6 (Artwork_6): Bottom component layer (signal_2), 0.5oz, Tz=50 ohm

3. Apply silkscreen on both side:
   Artwork_7: Top silkscreen.
   Artwork_8: Bottom silkscreen
4. Apply solder mask over bare copper on both side:
   Artwork_9: Top solder mask
   Artwork_10: Bottom solde mask
5. Material: FR4
6. Board thickness: 0.062'' +/- 0.010.
7. TRACE IMPEDENCE: 50 ohms +/- 10%.
8. See attached page for layer thickness specifications
9. Copper thickness 1oz before plating for all the power planes.
10. Copper thickness 0.5oz before plating for all the signal layers.
11. Ni/Au plating (3 to 8 micro-inches soft gold) over bare copper
12. All layers mininum trace width/clearence 0.007"/0.007"
13. All dimensions are in inches unless otherwise noted.

BOARD's DRILL SCHEDULE (Inch)

DRILL SYMBOL	DRILL SIZE	COUNT	PLATED	Min/Max
○	.015	365	YES	---
⊞	.02	15	YES	---
⦶	.028	8	YES	---
⊟	.035	40	YES	---
⊖	.041	150	YES	---
◫	.125	12	NO	---
⊕	.14	4	NO	---
□	.16	2	YES	---

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SCHM# B2523
SPEC# A2524
ASSM# B2525

UNIVERSITY OF CHICAGO
ELECTRONICS DEVELOPMENT GROUP

TITLE
A2524 Specification

SHEET 1 OF 1
DATE 05/08/2003
DRAWN TANG

B- 2524
REV 1.0